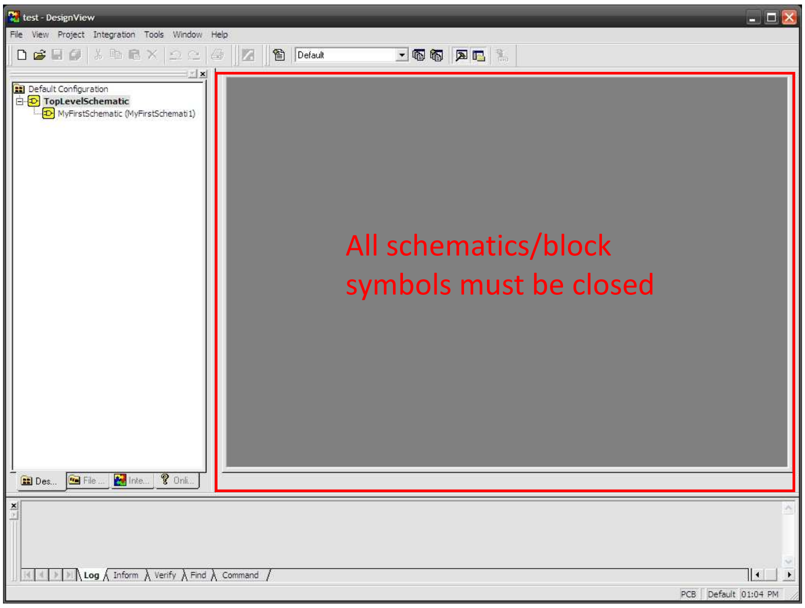
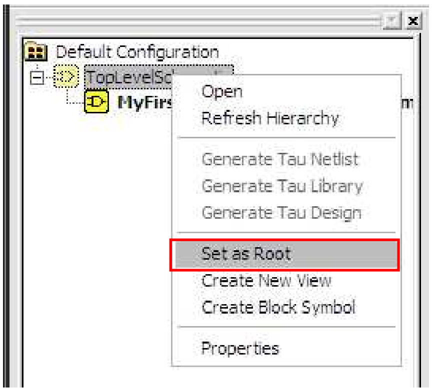
Expedition PCB Notes

Preparing a Schematic for PCB Layout

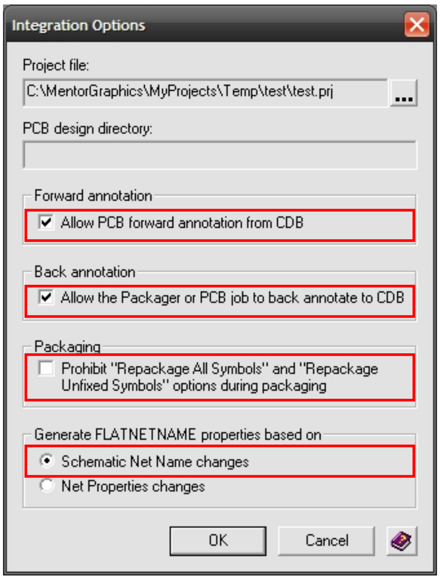
1. Open the project in DesignView, but do not open any schematic drawings or block diagrams. When configuring PCB related options or launching Expedition PCB from within DesignView, the main editor window *must* be empty (otherwise key schematic/layout integration functionality is silently disabled).



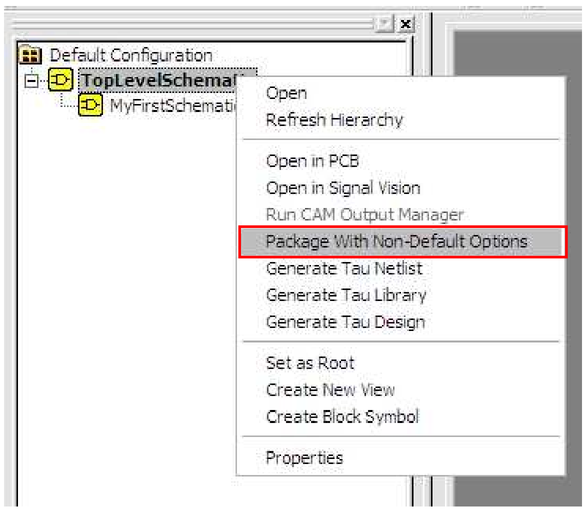
2. Ensure that the correct schematic is set as the top level design file for PCB generation. In almost all cases, this should be highest level entry in the 'Design Hierarchy' tab of the Project Manager side panel. Right click the schematic and select 'Set as Root'.



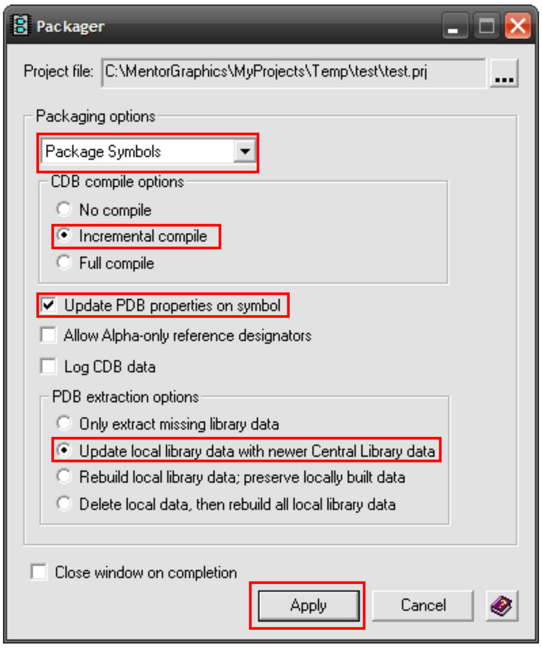
3. From the menu, select 'Project > PCB Integration…' to open the 'Integration Options' dialog. The 'Forward annotation' and 'Back annotation' options should be ticked, the 'Packaging' option should be unchecked and FLATNAME properties should be based on 'Schematic Net Name changes'.



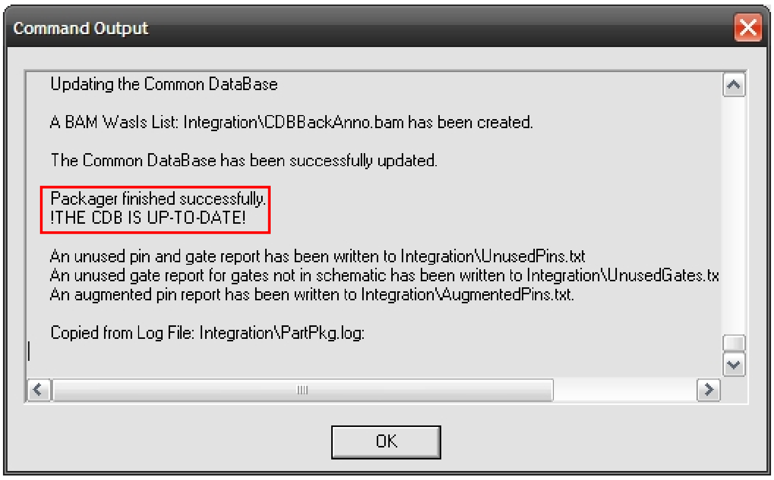
4. Before creating a layout, the various parts and net connections must be compiled into a format readable by Expedition PCB. This is done automatically when opening Expedition PCB, but since the default packaging options are sometimes inappropriate (e.g. when significant modifications have been made to the Central Library) it is good practice to perform manual compilations. Right click the top level schematic in the ‘Design Hierarchy’ tab of the Project Manager side panel and select ‘Package With Non-Default Options’ to open the ‘Packager’ window.



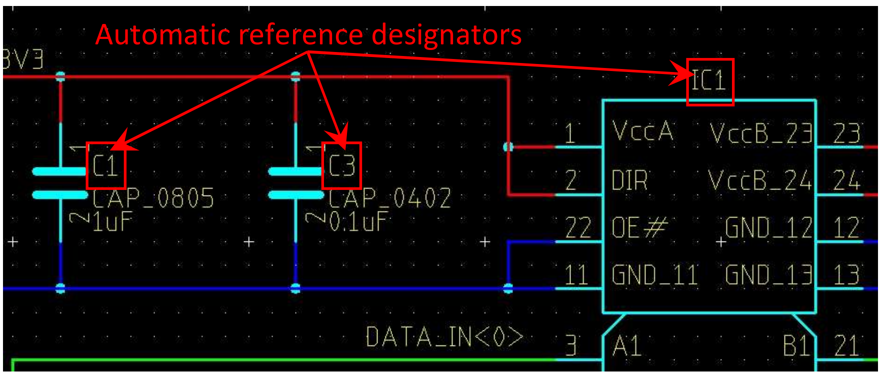
Under the ‘Packaging options’, select ‘Package Symbols’ (note that either of the ‘Repackage’ settings in this combo box will cause part reference designators to be reset – this is typically undesired behaviour). ‘CDB compile options’ should be set to ‘Incremental compile’, although specifying ‘Full compile’ will cause no harm (this simply forces a clean rebuild). In most cases, ‘PDB extraction options’ should be set to ‘Update local library data with newer Central Library data’; however, if several changes have been made to existing parts in the Central Library since the previous packaging operation, the ‘Delete local data, then rebuild all local library data’ option is recommended. ‘Update PDB properties on symbol’ should be the only box that is ticked. Click the ‘Apply’ button to proceed with compilation.



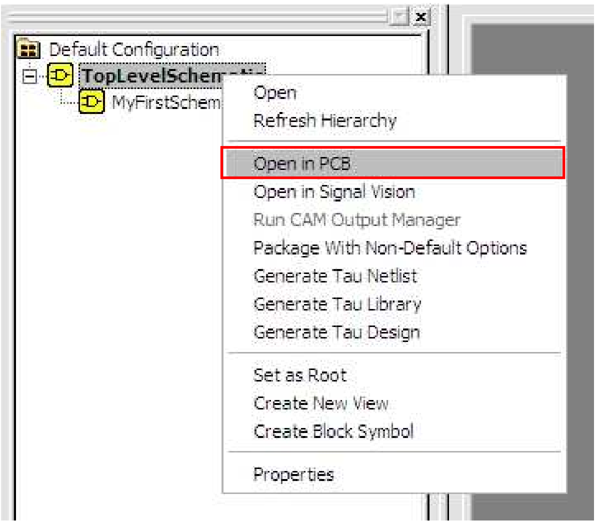
A log window will open. If there are any problems with the design, a descriptive error message will be displayed. Successful builds are indicated by the text: ‘Packager finished successfully. !THE CDB IS UP-TO-DATE!’



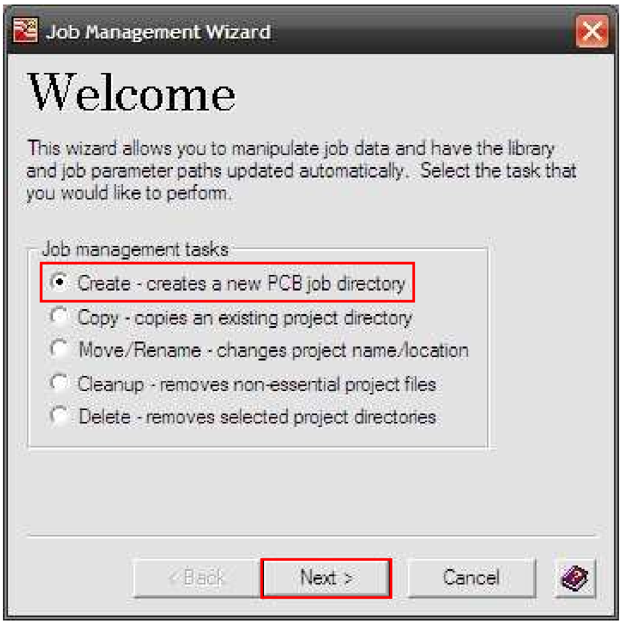
5. During packaging, reference designators will be assigned to all components that do not already have one. These are automatically added to the schematic drawings; if necessary, they should be repositioned for optimal readability.



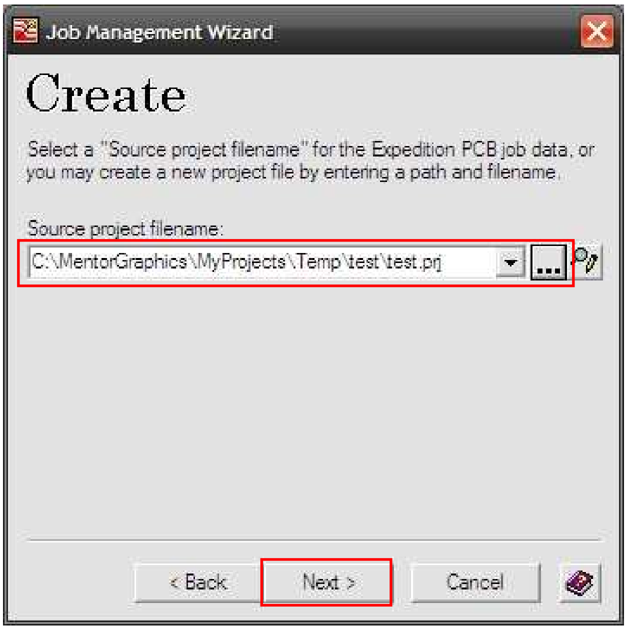
6. In order to commence PCB layout, right click the top level schematic in the design hierarchy (again ensuring that all schematic drawings and block symbols are closed) and select ‘Open in PCB’.



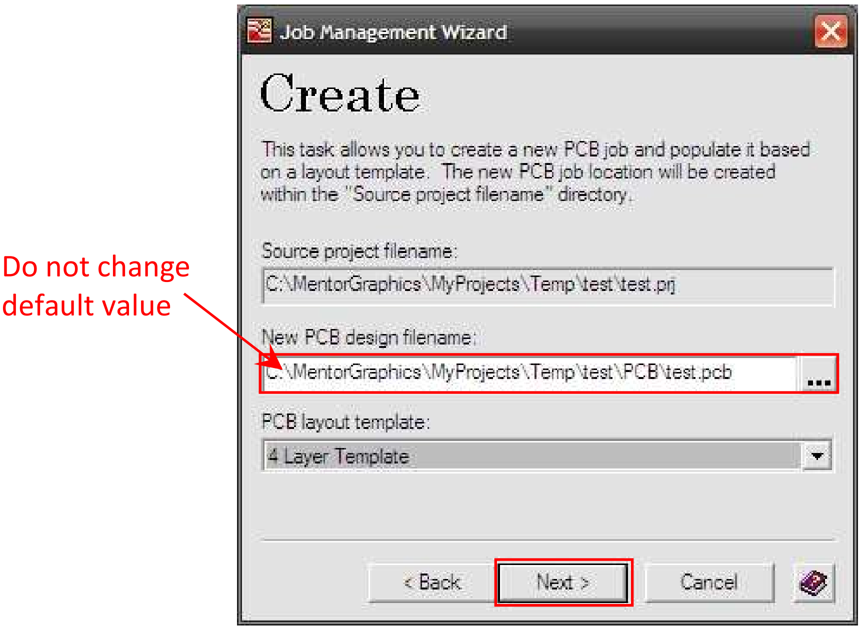
The first time that a schematic is opened in this fashion, the ‘Job Management Wizard’ will run (subsequent ‘Open in PCB’ operations launch Expedition PCB directly). Click ‘Create – creates a new PCB job directory’ and press the ‘Next >’ button to continue.



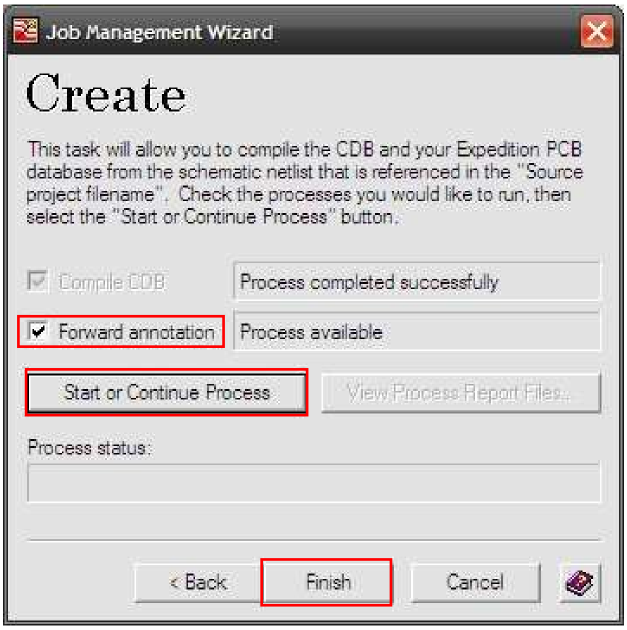
Click the ‘…’ button to open a file selection window. Choose the current project file (i.e. the ‘.prj’ file in the root project directory) and press ‘Next >’.



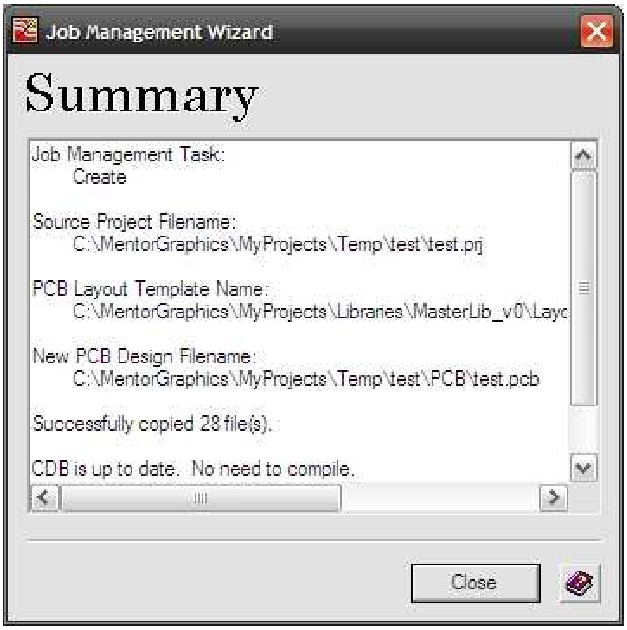
A ‘New PCB design filename’ will be generated automatically, and should not be changed. As with the DesignView ‘New Project Manager’, the ‘PCB layout template’ has only two options: ‘4 Layer Template’ and ‘8 Layer Template’. Again, the choice at this stage is not particularly important. Select whichever is closest to the planned design and click the ‘Next >’ button.



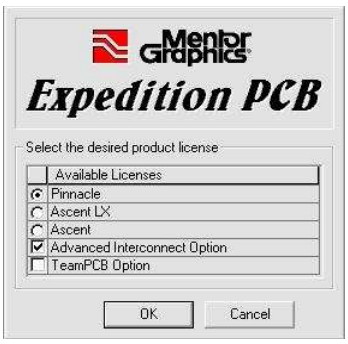
The final window is used to generate the PCB files. If the design was packed in accordance with Step 4 above, the ‘Compile CDB’ option will be greyed out. Ensure that ‘Forward annotation’ is ticked, and click ‘Start or Continue Process’. When the operation is complete, press the ‘Finish’ button.



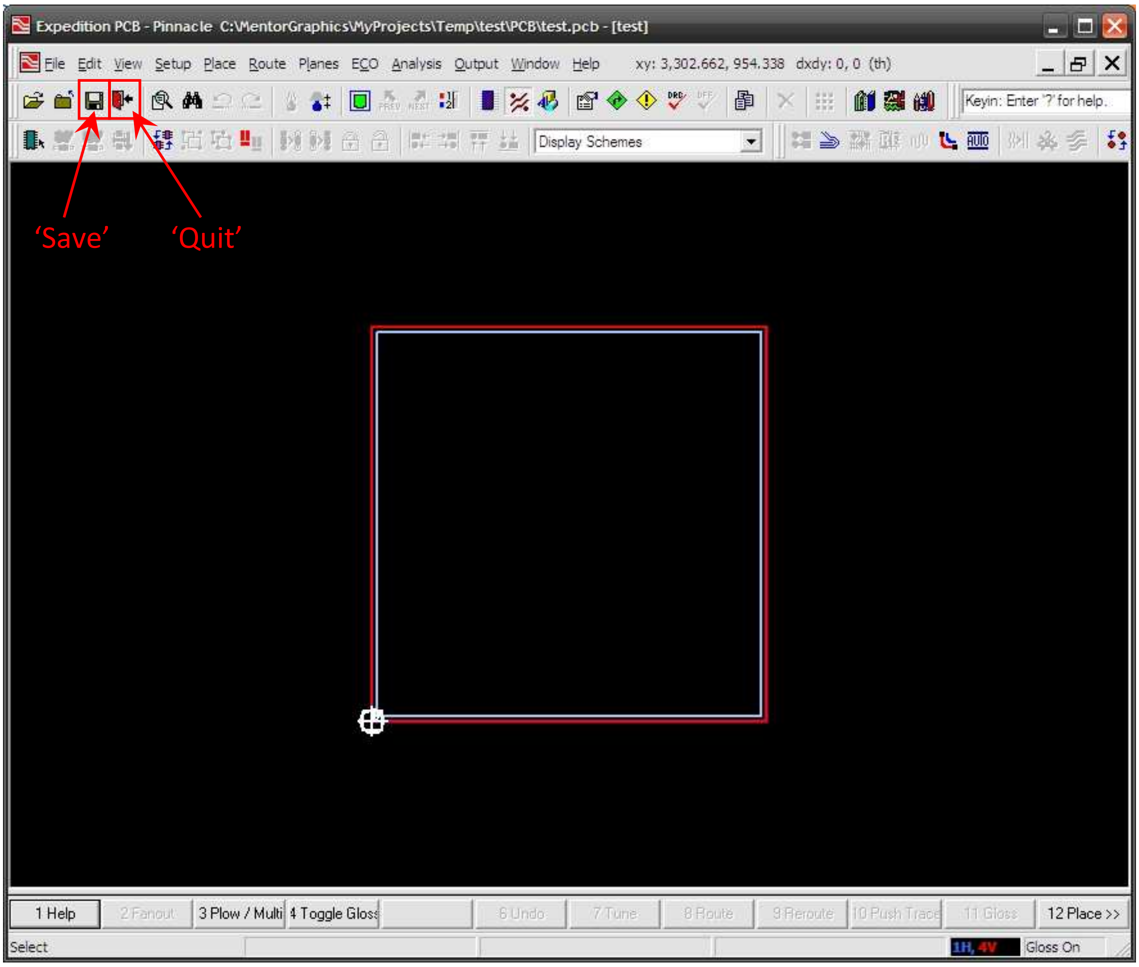
A summary panel will be displayed. Dismiss it with the ‘Close’ button, and Expedition PCB will launch.



7. When Expedition PCB opens, it will initially show a licence selection screen. There should be no need to change any settings here, so either press the ‘OK’ button or just wait a few seconds and it will close automatically.



The main Expedition PCB editor window will then be displayed, with a default empty board outline filling the screen. In theory, layout may now commence – however, it is not possible to produce a manufacturable PCB until further information has been obtained. Consequently, save the initialised design (via the 'Save' button) and close the editor (via the 'Quit' button).



Collecting Manufacturing Information

A PCB cannot be designed without a complete knowledge of manufacturing limitations and physical material properties. The only sources of this information are PCB manufacturers. Since each manufacturer utilises different production techniques/equipment/materials, their physical constraints are often unique. A PCB that has been designed following the guidance of a particular manufacturer cannot necessarily be produced by any other manufacturer (without significant reworking).

It is therefore important to choose a manufacturer as soon as possible in the design process, and to avoid switching manufacturers during a project. For MICE UK work, **Express Circuits Ltd** (http://www.express-circuits.co.uk) are recommended; they produce high quality results and are very cost effective.

The first aspect to consider when laying out a PCB is 'Design For Manufacture' (DFM) – i.e. principles for reducing the cost and difficulty of making the board. Designs with the fewest layers and the largest features (holes, tracks, hole/track spacings, etc.) are cheapest and quickest to produce, and all manufacturers have hard limits on the smallest feature sizes that are physically achievable. Some companies produce detailed DFM documents; **Express Circuits Ltd** simply states a list of manufacturing capabilities on their website:

- Max Brd Dimensions - 550 x 480mm
- Max Brd Thickness - 4.8mm
- Number of Layers - Max 28 layers
- Min Track: - 75 microns (^{3}50 micron in controlled areas)
- Min Gap: - 75 microns (^{3}50 micron in controlled areas)
- Smallest Mechanical Hole: - 0.1mm Drilled (PCB Thickness Dependant)
- Smallest Laser Hole: - 0.05mm Finished (Layer Separation Dependant)
- Aspect Ratios: - 8:1 Drilled (Dependant)
- Hole to Copper - 0.15mm (Design dependant)
- Controlled Impedance - +/-10% Standard or +/-5% Advanced
- Copper Filled Vias - Flat Pad Technology

If possible, it is wise to at least double the minimum track and gap (unless using controlled impedance), smallest hole and hole-to-copper dimensions when planning a design.

Controlled impedance is recommended for most signalling tracks. It is not required for low frequency signals, but since it effectively adds nothing to the cost of a board there is little reason to forgo the increased reliability that it offers. The most common types of controlled impedance are:

- 50Ω single ended
- 100Ω differential

Controlled impedance values determine the track widths and gaps that should be used on each layer of a board. In general, these track dimensions cannot be calculated by the designer – they must be obtained from the manufacturer. When requesting this information, the following must be provided:

- Number of layers
- Board thickness *(in mm)*
- Laminate material
- For each layer:
    - Plane type *(signal or power/ground)*
    - Copper weight *(in oz)*
    - Which types of controlled impedance tracks are present

A number of the above parameters have standard values that should be appropriate for all MICE PCB builds:

- Board thickness: 1.6 mm
- Laminate material: High Tg FR4 (Required for lead free designs – i.e. anything using components less than a few years old)
- Copper weight: ½ oz (1 oz copper is sometimes appropriate for power/ ground planes)

For reference, an example of the type of email request that should be sent to a manufacturer is given below:

```
I would be grateful if you could provide track and gap widths for the following
8 layer build:

Layer 1:  signal       (1/2 oz copper)
Layer 2:  GND plane    (1/2 oz copper)
Layer 3:  signal       (1/2 oz copper)
Layer 4:  power plane  (1 oz copper)
Layer 5:  power plane  (1 oz copper)
Layer 6:  signal       (1/2 oz copper)
Layer 7:  GND plane    (1/2 oz copper)
Layer 8:  signal       (1/2 oz copper)

Board thickness: 1.6 mm
Laminate: High Tg FR4
Signal tracks: All 50 ohm single ended
```

Track/gap widths provided by a manufacturer are entirely dependent on layer stackup. Consequently, it is essential (if at all possible) to fix the structure of a PCB before commencing layout; if it is necessary to change the number of layers or layer types partway through a design, it is almost inevitable that all existing tracks will have to be ripped up and rerouted.

Defining PCB Layer Stackups

A PCB stackup may be defined in a multitude of ways, but the following rules must be obeyed:

- Stackups must contain an even number of layers
- Stackups must be symmetric (i.e. the ordering of signal and power/ground planes must be mirrored about the centre)
- Signal planes must never be placed on adjacent layers

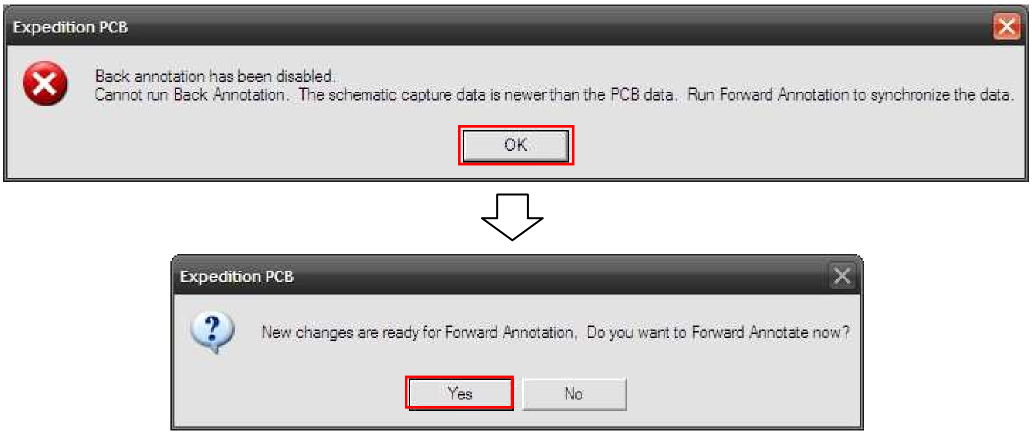
The following guidelines should also be observed in order to maximise the quality of the final result:

- Place a ground plane next to the surface layer (i.e. top or bottom) upon which are mounted the highest number of components. If possible, place a ground plane next to both surface layers (the goal is to minimise the length of the current path between each component and ground)
- Where possible, place analogue signal planes next to analog power/ground planes (and digital signals next to digital power/ground planes)
- It is OK (and common) to place additional power/ground plane shapes on signal layers; it is not OK to place signal tracks on power/ground planes (even if it's just a single track, and you are sorely tempted due to lack of space…)
- If possible, use a separate plane for each ground and power voltage level. In cases where this is not financially viable (many layers = high cost), it is acceptable to split power planes into a number of subsections at different voltages. Splitting of ground planes should be avoided
- When using split power planes, do not route tracks in any adjacent signal planes across the split boundaries

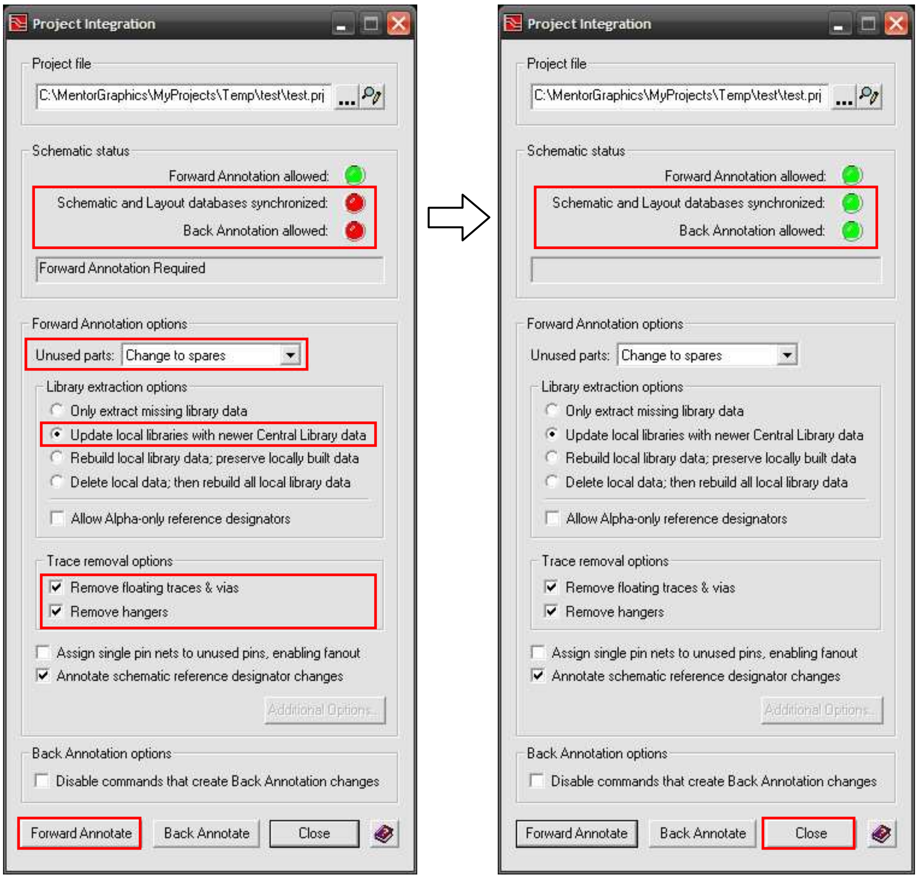
Configuring Board Parameters in Expedition PCB

1. Open the project in DesignView. *Ensure that all schematic drawings and block symbols are closed*. Right click the top level schematic in the 'Design Hierarchy' tab of the Project Manager side panel and select 'Open in PCB'.

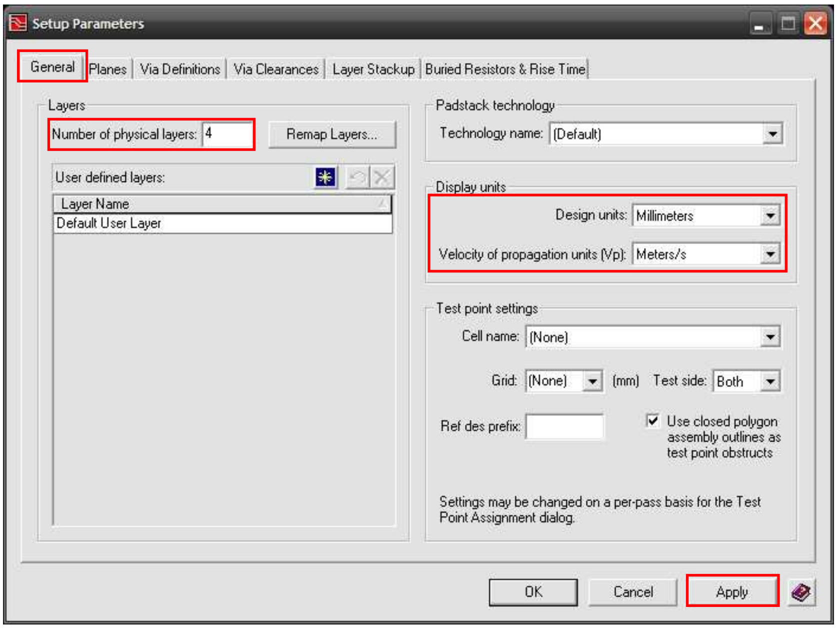
2. If any changes have been made to the design at the schematic level, Expedition PCB will display a warning dialog that states 'Back annotation has been disabled'. Click the 'OK' button and a second dialog will appear, enquiring 'Do you want to Forward Annotate now?'. Open the 'Project Integration' window by clicking the 'YES' button. *(NB: The user is sometimes required to go through this process when reopening a project in Expedition PCB even if no changes have been made – DesignView has a habit of automatically updating the timestamp on certain system files, and these modifications can trigger a forward annotation request in the same manner as user edits)*



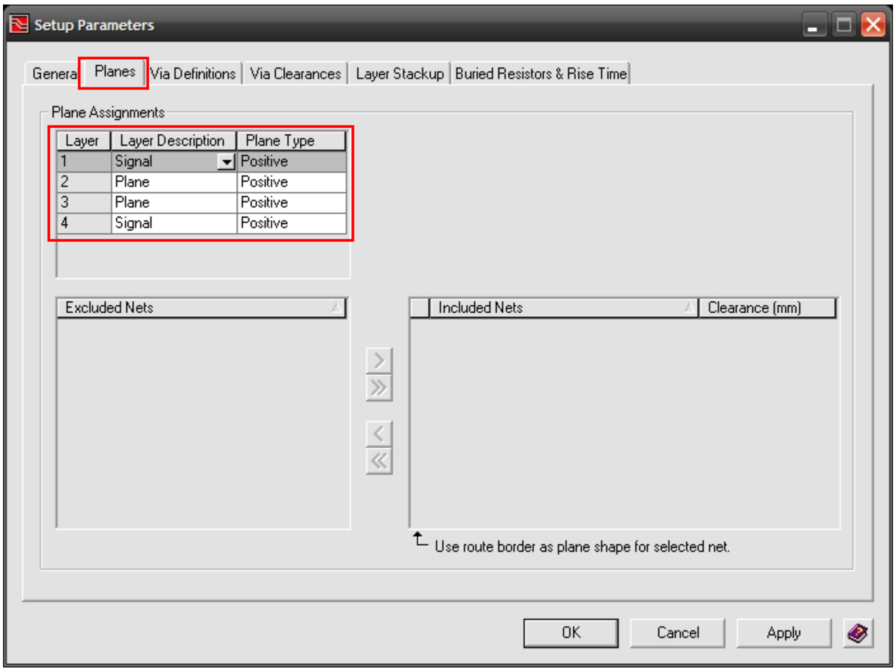
In the Project Integration window, set 'Unused Parts' to 'Change to spares' and select 'Update local libraries with newer Central Library data' in the 'Library extraction options' section. Ensure that both 'Trace removal options' are ticked, and click the 'Forward Annotate' button. When the operation is complete, the 'Schematic status' indicators should all turn green. Press the 'Close' button to dismiss the window.



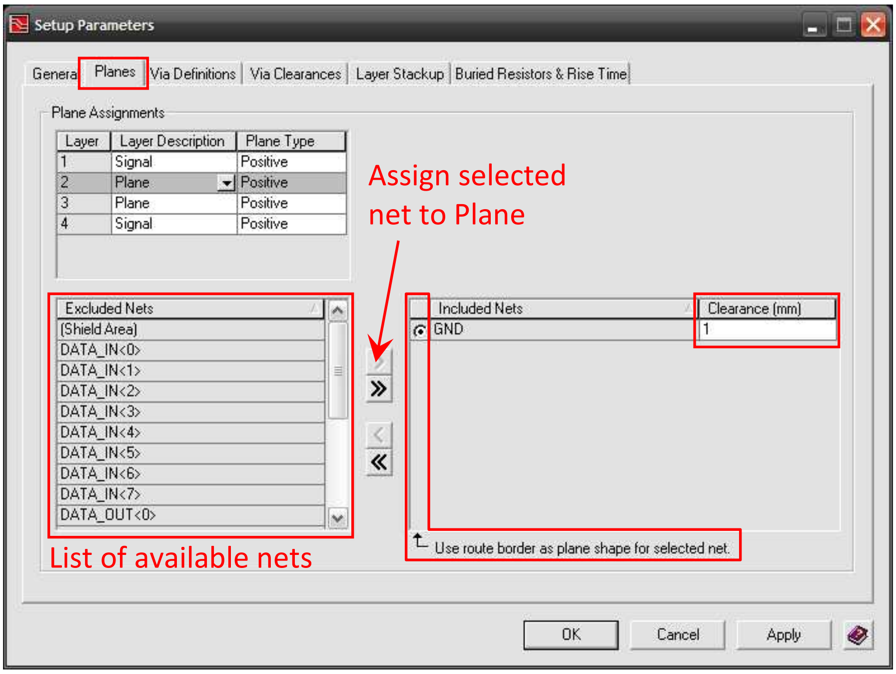
3. PCB configuration may now begin. Select 'Setup > Setup Parameters…' from the menu to open the 'Setup Parameters' dialog. In the 'General' tab, enter the 'Number of physical layers' that should be included in the PCB stackup. Set 'Design units' to 'Milimeters' and 'Velocity of propagation units' to 'Meters/s', then click the 'Apply' button.



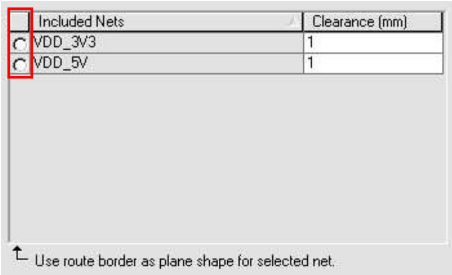
In the 'Planes' tab, use the 'Plane Assignments' table to define the properties of the PCB stackup. From the drop down menus in the 'Layer Description' column, configure each layer as either 'Signal' (for a signal plane) or 'Plane' (for a power/ground plane). Power/ground planes should be given a 'Plane Type' of either 'Positive' or 'Negative', depending on their voltage levels (note that 'ground' is always defined as 'Positive').



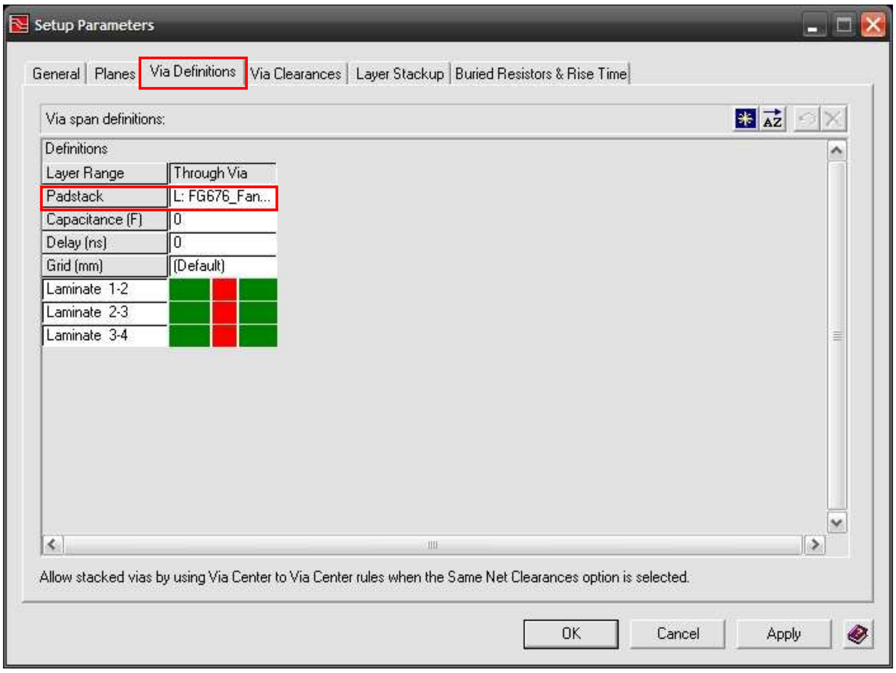
Each 'Plane' layer must be assigned at least one net. Select the layer in the 'Plane Assignments' table and a list of all available nets will appear under the 'Excluded Nets' heading. Highlight the required net(s) and click the '>' button to attach them to the plane. If a plane has a single net, the 'Use route border as plane shape for selected net' option should be enabled. Plane 'Clearance' (i.e. the minimum allowed spacing between plane shapes for different nets) should typically be set to 1 mm.



For split power planes containing multiple nets, disable the 'Use route border as plane shape for selected net' option – the individual plane shapes must be drawn by hand (this is discussed in a later section of the document).

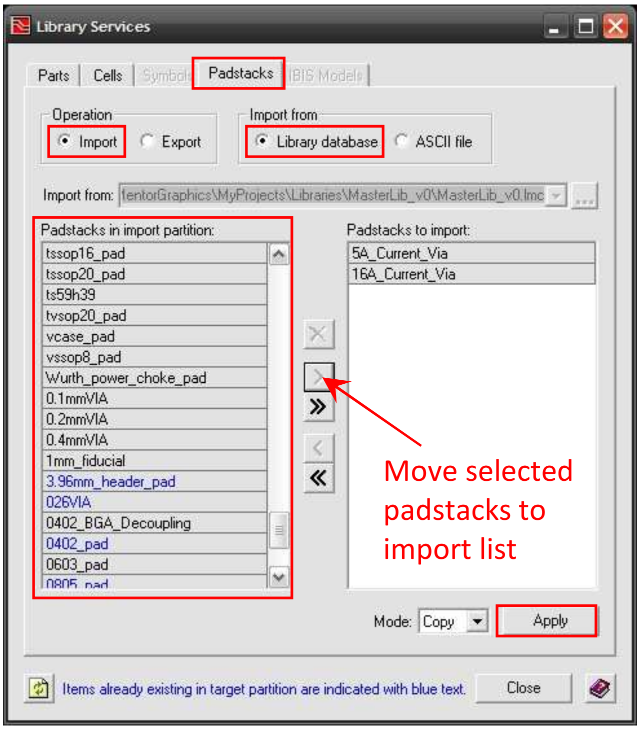


By default, in the 'Via Definitions' tab there will be a single 'Through Via' span definition. It should only be necessary to set the 'Padstack' here, which will become the default via padstack for all routing operations. Click the padstack name entry and a drop down menu will appear containing all the via padstacks defined in the Central Library; the **FG676_Fanout_Via** (despite its component specific name) is a good choice for all standard designs. It is also possible to define additional via spans that only connect certain layers of a PCB (rather than passing all the way through), but this is strongly discouraged. These 'blind vias' are sometimes useful for very dense, tightly packed layouts, but they will be prohibitively expensive for any MICE work.

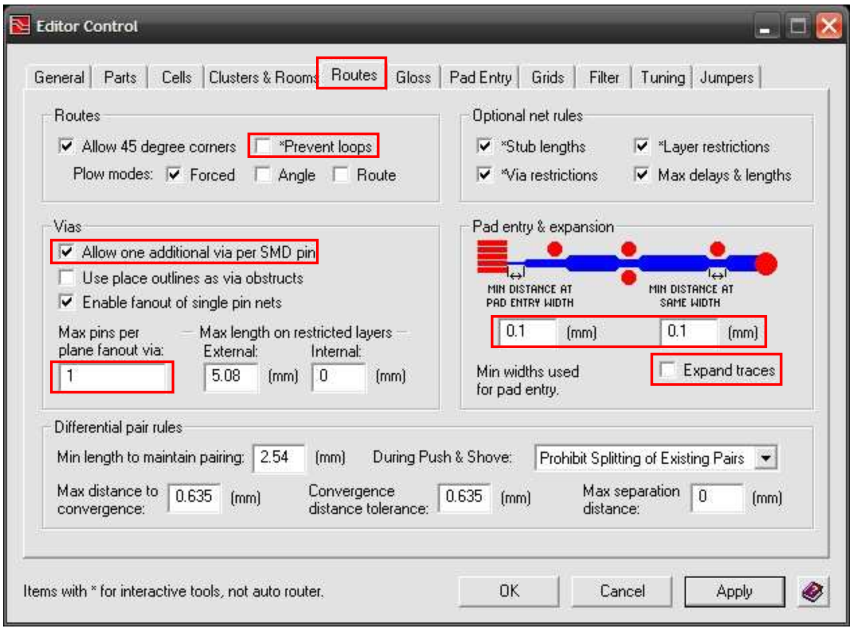


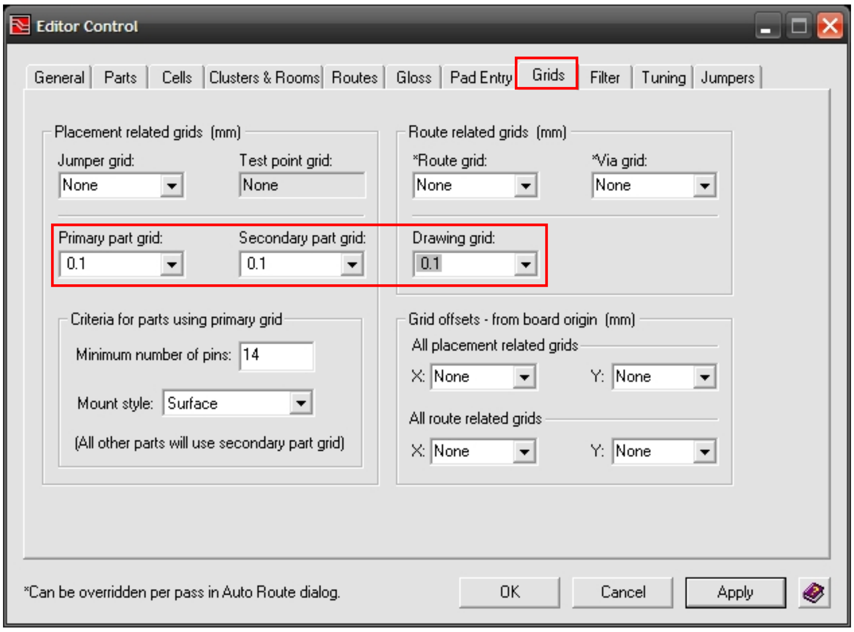
All other tabs of the 'Setup Parameters' dialog may be left with their default settings – press the 'OK' button to close the window.

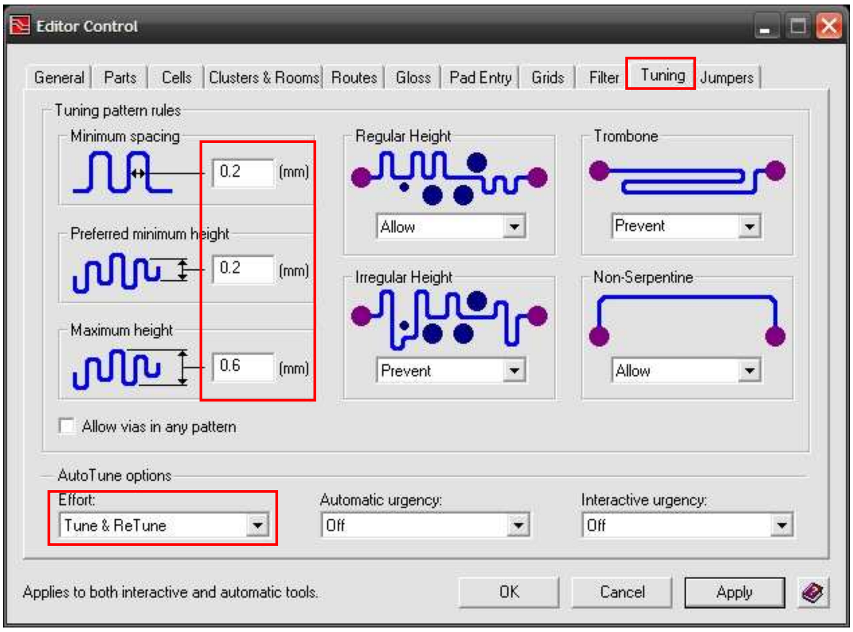
Note: The default padstack specified in the 'Via Definitions' tab is automatically imported into the local Expedition component library. If it is necessary to use other via padstacks for specific nets (e.g. a large via may be required where a board has high current power tracks), they must be imported manually. In order to do this, select 'Setup > Library Services…' from the menu to open the 'Library Services' dialog. Go to the 'Padstacks' tab, highlight the desired entries in the 'Padstacks in import partition' list, click the '>' button to move them to the 'Padstacks to import' list and press the 'Apply' button before closing the window.



4. Select ‘Setup > Editor Control…’ from the menu to open the ‘Editor Control’ dialog. Many of the options here are somewhat subjective and design dependent. However, the following screenshots show recommended settings that should be appropriate for most standard layouts.

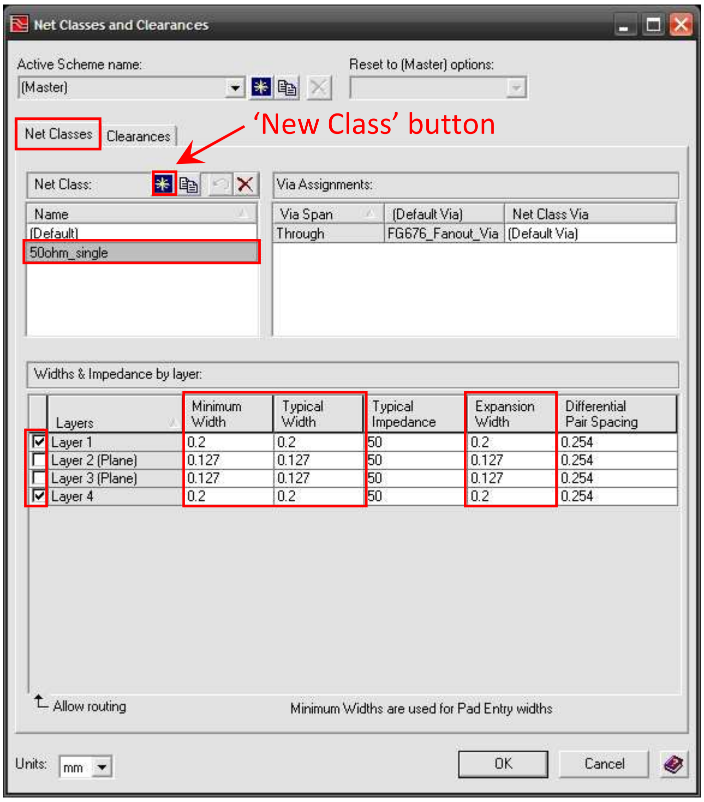






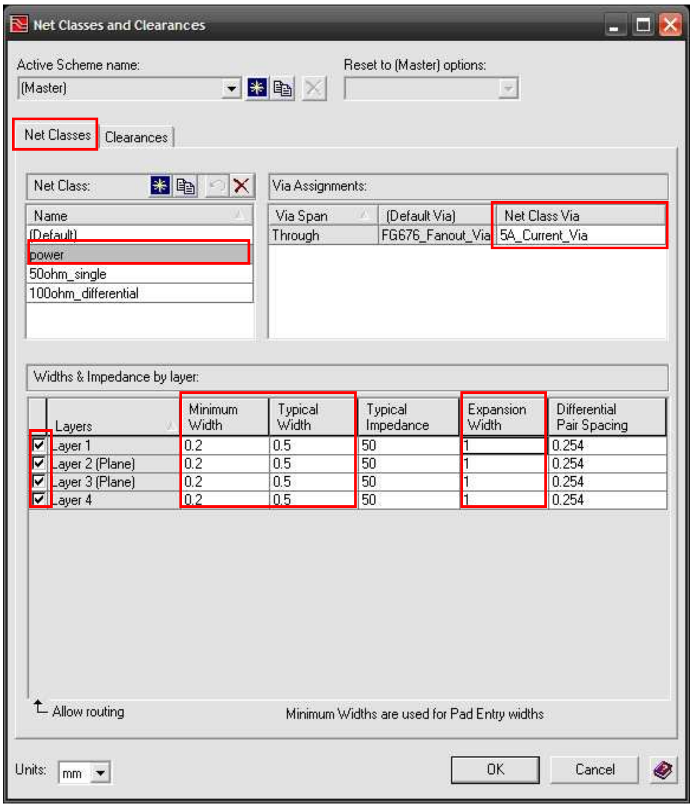
Note that any tab not represented among the above screenshots may be ignored. Click the ‘OK’ button to close the window.

5. Select ‘Setup > Net Classes and Clearances…’ from the menu to open the ‘Net Classes and Clearances’ dialog. This is used to create rules for the widths and spacing of routed tracks. For example, to set up a class definition for controlled impedance 50Ω single ended signals go to the ‘Net Classes’ tab, click the ‘New Class’ button and enter the name ‘50ohm_single’ (or any other appropriate identifier). Ensure that the class is highlighted in the ‘Name’ list and enter the track widths obtained from the manufacturer in the ‘Minimum Width’, ‘Typical Width’ and ‘Expansion Width’ columns of the ‘Widths’ table. *Note that all three columns must be identical for controlled impedance tracks*. When defining a class for differential tracks, the ‘Differential Pair Spacing’ column must also be filled with manufacturer data, otherwise it should be ignored (the ‘Typical Impedance’ column should always be ignored). For signal tracks, it is best practice to uncheck the ‘Allow routing’ box for any Plane layers.

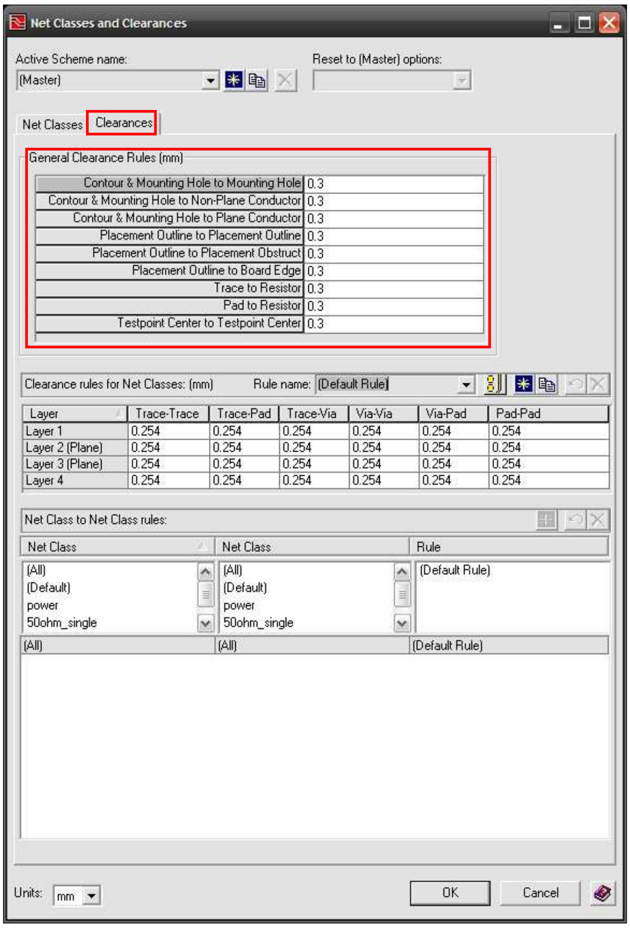


Classes for power nets (and perhaps certain slow analogue signals, e.g. voltage references) are slightly different from those for controlled impedance, in that the track widths should be determined from the current they are expected to carry. These values should be entered in the ‘Typical Width’ column, which is used for all standard routing operations. In practice, the ‘Minimum Width’ column indicates the width that a track may shrink to as it enters the padstack of a component; minimum widths should always be set to a value comparable with ordinary single ended data signals – if they are too large (i.e. greater than the pin spacing of the smallest component on the PCB), it will be physically impossible to route the track to a device (as it would overlap multiple unrelated pins). The ‘Expansion Width’ is the maximum width that a track may have. With the above ‘Editor Control’ configuration it will never be used automatically while routing, but it may be selected as a manual override; this can be useful if it is ever necessary to draw a particularly long instance of a power track (since required track width for a fixed current increases with length).

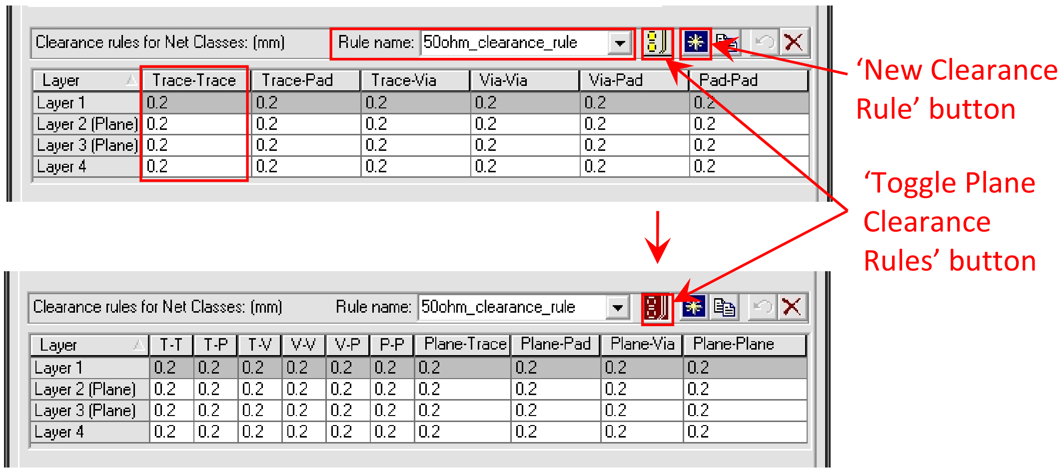
It is also possible to set an alternative via for each class by clicking the ‘Net Class Via’ entry. This is primarily used to specify larger vias for high current nets. Either the ‘Net Class Via’ or the global ‘default’ via may be selected while laying a track (this is discussed in a later section of the document).



Once all classes have been defined, select the ‘Clearances’ tab. The ‘General Clearance Rules’ should be derived from the manufacturer’s DFM guidelines. If in doubt, 0.3 mm is typically a ‘safe’ value for all of these entries.



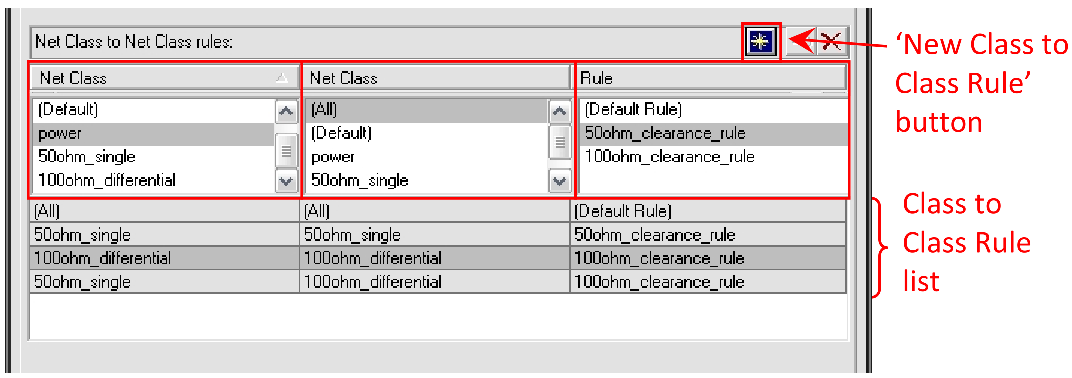
It is then necessary to create class specific clearance rules. Click the 'New Clearance Rule' button, enter an appropriate name (typically some derivative of the associated class name, with a 'rule' suffix) then fill the clearances table. *Note that the 'Toggle Plane Clearances Rules' button must be pressed in order to reveal all of the columns*. For controlled impedance signals, place the gap widths obtained from the manufacturer into the 'Trace-Trace' column; other signals should typically have 'Trace-Trace' spacing equal to their minimum track width, although larger values may be used for high current tracks to avoid the risk of shorting due to heat expansion. The remaining columns should be derived from DFM guidelines – however, in most cases it is generally acceptable to reuse the 'Trace-Trace' values.



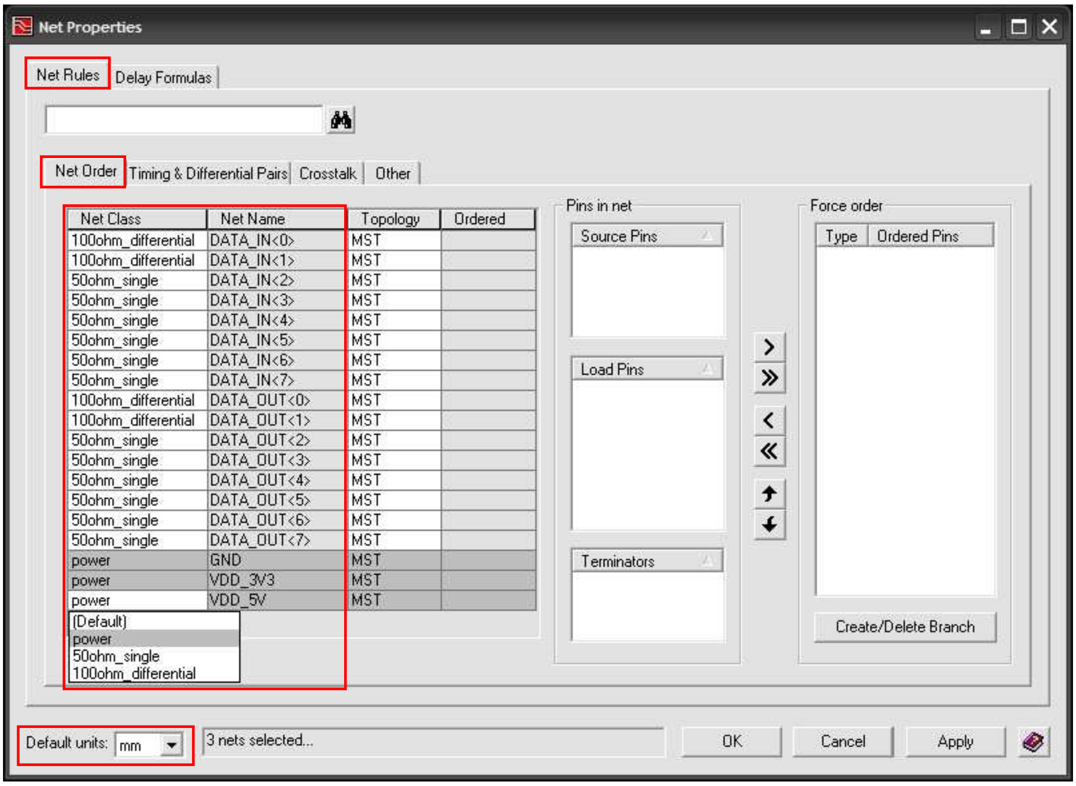
The final step is to link net classes to clearance rules. At the bottom of the dialog window highlight a class from each of the 'Net Class' columns and a clearance rule from the 'Rule' column, then press the 'New Class to Class Rule' button. Repeat this for each net class, as required. In the following screenshot example, four rules have been created:

A. The spacing between '(All)' nets will be specified by the '(Default Rule)'
B. The spacing between '50ohm_single' class nets will be specified by the '50ohm_clearance_rule'
C. The spacing between '100ohm_differential' class nets will be specified by the '100ohm_clearance_rule'
D. The spacing between '50ohm_single' class nets and '100ohm_differential' class nets will be specified by the '100ohm_clearance_rule'

For instances where rules conflict, those which specify a particular net class will override those which refer to '(All)' nets – i.e. B, C and D will always override A.

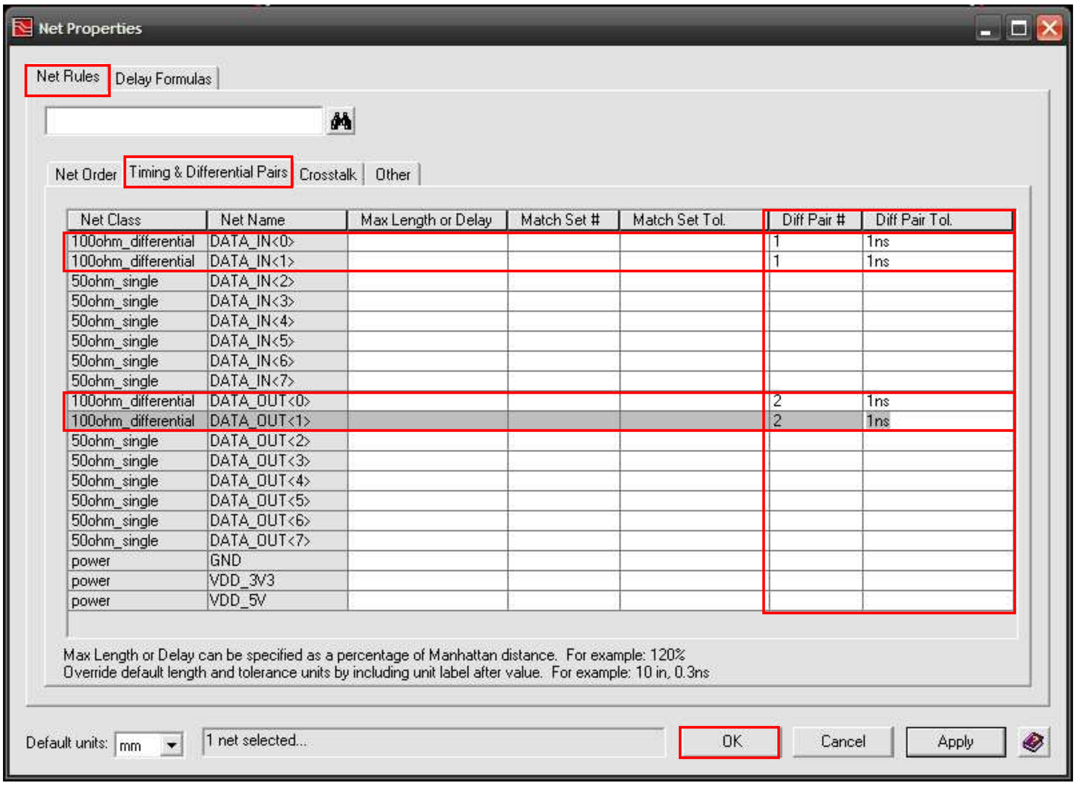


6. Once all classes have been defined, it is necessary to assign them to the individual nets in the design. Select ‘Setup > Net Properties…’ from the menu to open the ‘Net Properties’ dialog and go to the ‘Net Rules’ > ‘Net Order’ tab. Ensure that ‘Default units’ is set to ‘mm’. Clicking on any entry in the ‘Net Class’ column of the table produces a drop down menu from which a class may be selected; multiple nets may be configured at once by highlighting them and holding the SHIFT key while accessing the drop down menu.

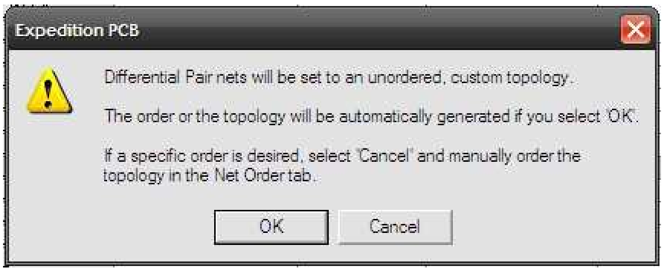


If the design utilises differential signalling, go to the ‘Net Rules’ > ‘Timing & Differential Pairs’ tab. For the nets that form each differential pair, enter a unique ‘pair index’ in the ‘Diff Pair #’ column. The ‘Diff Pair Tol.’ column sets the maximum allowed total length difference between the two tracks of a differential pair (values may be specified in units of either distance or signal propagation time).

This tab may also be used to identify groups of nets which must have the same length/propagation delay, by assigning a ‘group index’ in the ‘Match Set #’ column and a maximum allowed track-to-track length/delay deviation in the ‘Match Set Tol.’ column. However, this is only relevant for specialised applications (e.g. very high speed QDR RAM signalling) – it is unlikely that the option will ever be required for MICE work.



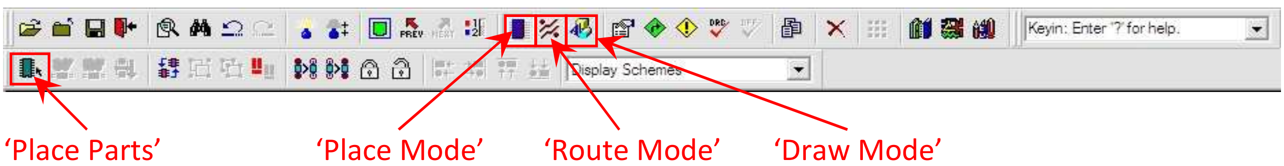
If any differential pairs have been set, clicking the ‘OK’ button to close the dialog will generate the following pop up warning message:



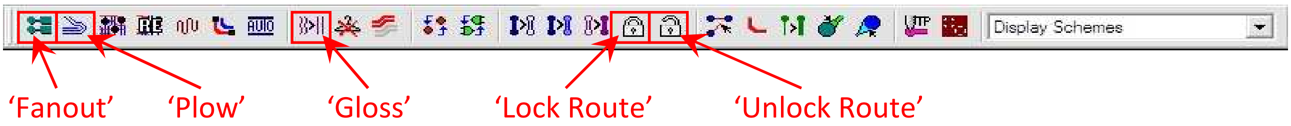
In most cases, this may be ignored – simply click the ‘OK’ button and then close the ‘Net Properties’ window. It is now possible to commence layout of the PCB.

The Expedition PCB Toolbar

The following notes make a number of references to buttons on the Expedition PCB toolbars; these are highlighted in the screenshots below:



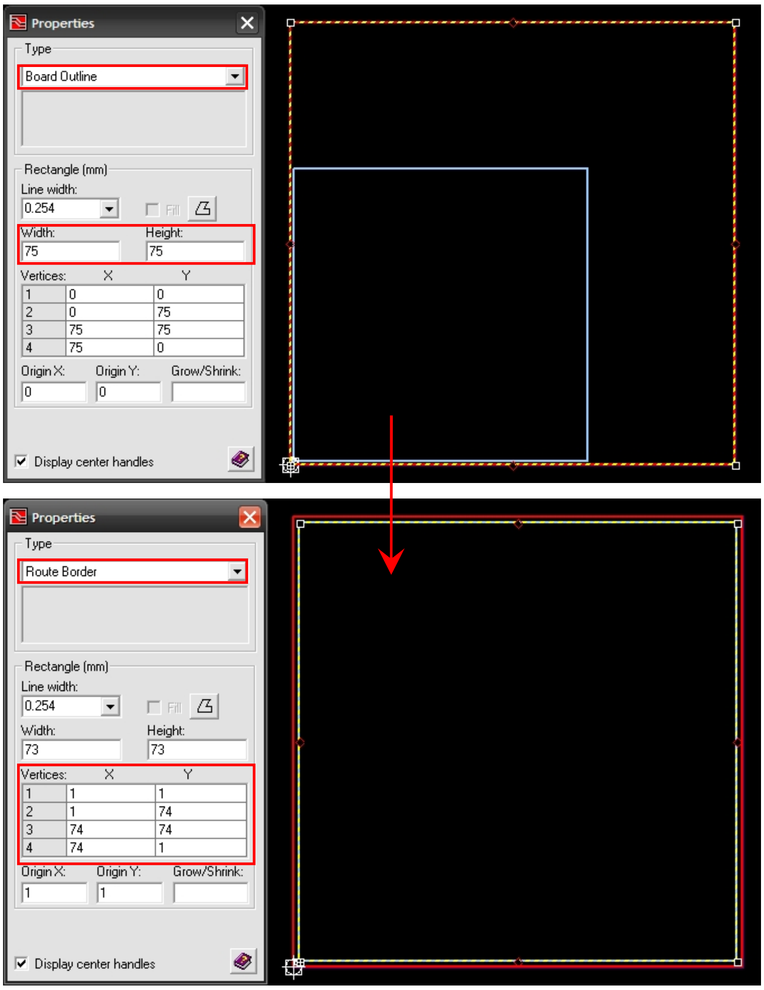
When the ‘Route Mode’ button is pressed, an additional toolbar is shown:



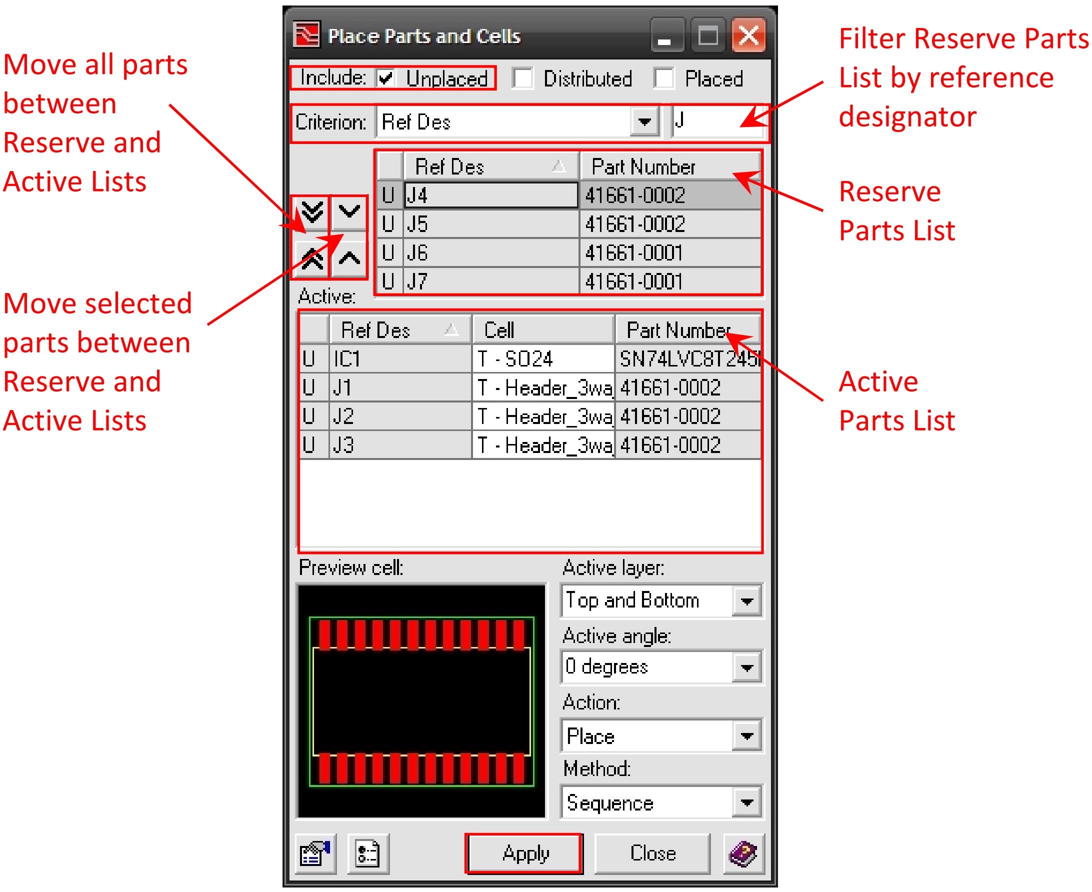
Clicking the ‘Draw Mode’ button shows another additional toolbar:

Laying Out A PCB

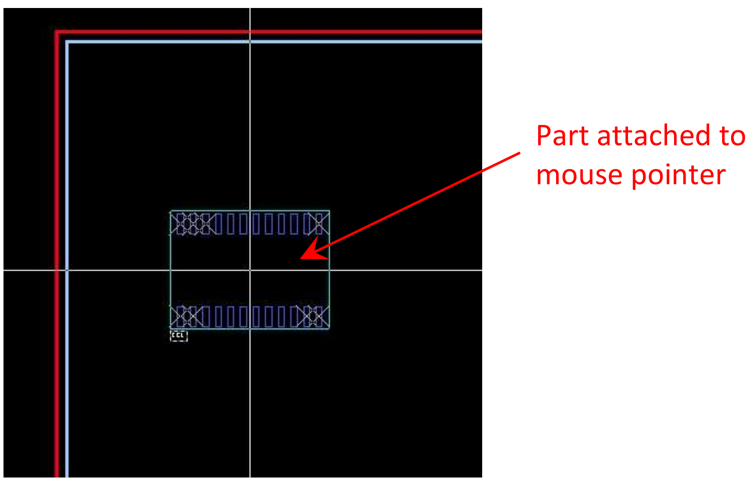
1. When a PCB project is created, the board is given a default size of 50 x 50 mm. To change this, click the ‘Draw Mode’ button in the toolbar and double click the red ‘Board Outline’ to open the ‘Properties’ dialog. Enter an appropriate ‘Width’ and ‘Height’ to define the physical area of the board. Click on the blue ‘Route Border’ and use the ‘Vertices’ table to define a region inside the ‘Board Outline’ with a clearance of at least 1mm on all sides *(NB: the absolute minimum manufacturing limit for this clearance is 0.254mm)*. Tracks and plane shapes may only be placed within the ‘Route Border’ – having a 1mm gap between the edge of the PCB and any copper areas minimises the risk of exposing layers through the laminate and introducing short circuits between them (this can happen when the board is cut out during fabrication).



2. Once the board shape has been specified, individual components may be placed. Click the ‘Place Mode’ button on the toolbar, followed by the ‘Place Parts’ button to open the ‘Place Parts and Cells’ dialog. Tick the ‘Include’ ‘Unplaced’ checkbox and a list of all available components will be displayed in the ‘Reserve Parts List’; this may be filtered (typically by reference designator) using the ‘Criterion’ options. Use the ‘>’ or ‘>>’ buttons to move items from the ‘Reserve Parts List’ to the ‘Active Parts List’, and click the ‘Apply’ button.

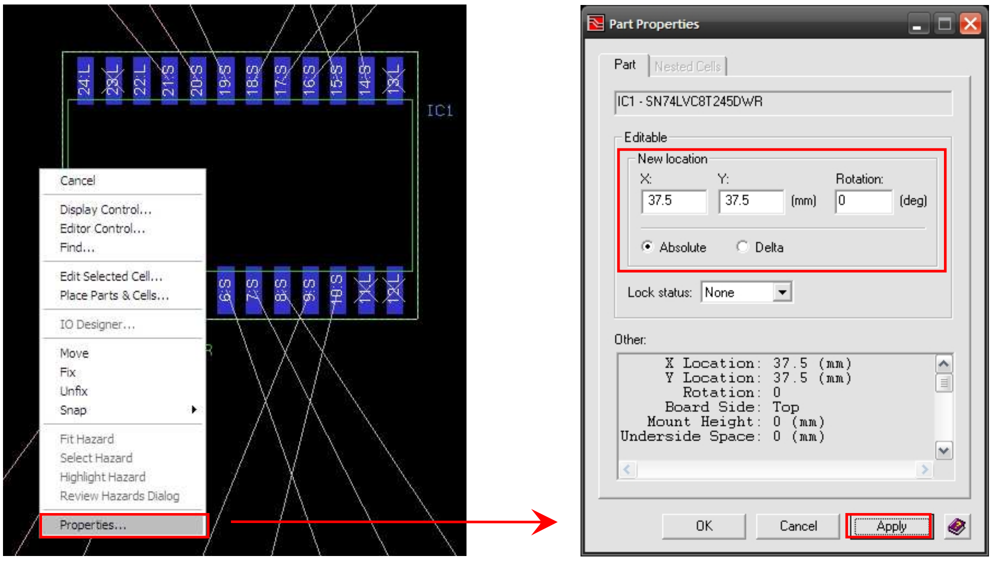


The first item in the ‘Active Parts List’ will be attached to the mouse pointer and it may be placed by clicking anywhere on the PCB; this should be repeated for each of the other items in turn, until the ‘Active Parts List’ is empty (at which point the dialog may be closed).



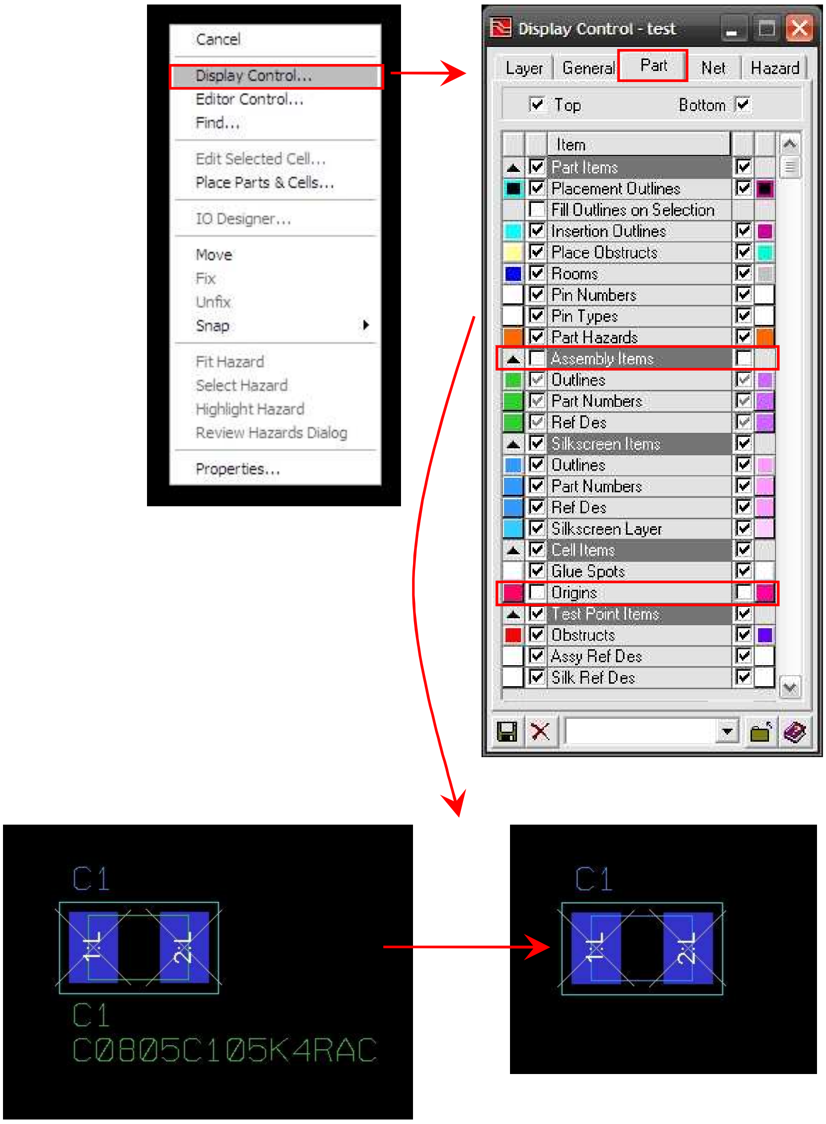
The ‘Function Bar’ at the bottom of the screen is invaluable when positioning components. To move a part that has been placed, highlight it and press the ‘Move’ button – it will be reattached to the mouse pointer and may be placed with another click. The ‘Rotate’ buttons will rotate the currently selected part, and the ‘Push’ button transfers the component between the top and bottom layers of the board. Note that each of the ‘Function Bar’ buttons is mapped to the correspondingly numbered Fn key on the keyboard. Selected components can also be moved with the cursor keys.

To set the location of a placed part with greater accuracy, right click it and select ‘Properties…’ to open the ‘Part Properties’ dialog. Enter the required coordinate values in the ‘New Location’ box and press the ‘Apply’ button.

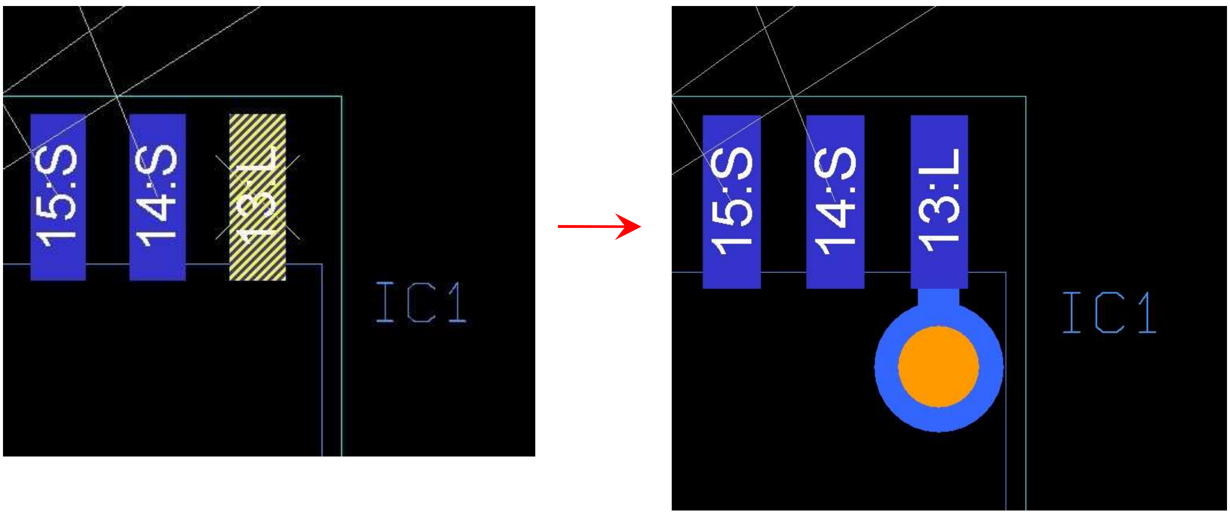


3. By default, the assembly information associated with each component is displayed within the PCB editor. This text is entirely irrelevant for layout purposes and just serves to clutter up the screen. To switch it off, right click anywhere on the PCB and select ‘Display Control…’. In the ‘Display Control’ window, go to the ‘Part’ tab and uncheck the ‘Assembly Items’ entry (this should be done on both the left and right hand sides of the control, which correspond to the top and bottom of the board). The ‘Origins’ entry should also be unchecked.

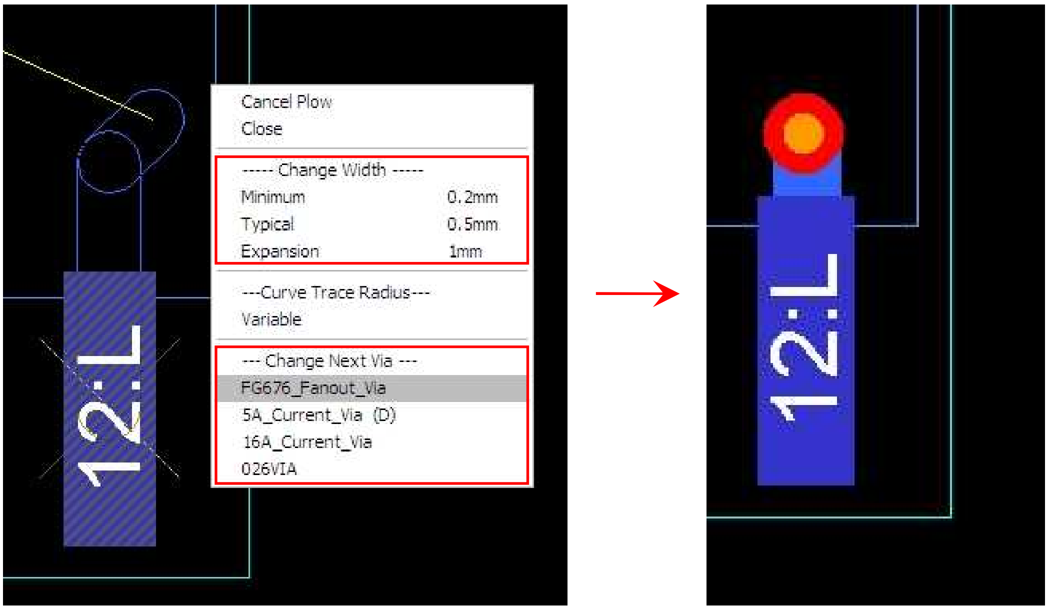
   The ‘Display Control’ window is frequently of use when routing a PCB; it is recommended to keep it open at all times.



4. Once components have been placed, it is normal to initially fan out any surface mount pins that should be connected to power/ground planes (these pins can be identified by the white crosses which pass through their centres). To do this in an automated fashion, click the ‘Route Mode’ button on the toolbar, click to highlight the required pin and press the ‘Fanout’ button (also on the toolbar). Provided that there is sufficient space around the affected component, a default net class via will be placed and routed to the pin.

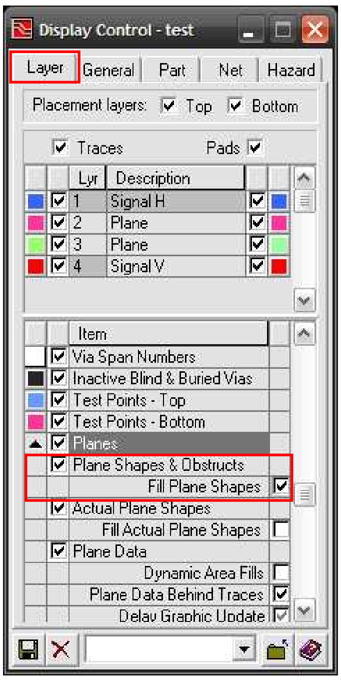


If greater control is required, fanouts may also be performed manually. Highlight the required pin and click the ‘Plow’ button on the toolbar. The mouse pointer will turn into a track outline which can be moved freely across the PCB. Right clicking will open a menu from which it is possible to change the width of the track to any of the values entered in the Minimum, Typical or Expansion Width columns when specifying the net class; this menu can also be used to override the default net class via with any via padstack referenced in the design. To place the fanout via, simply double click in any free space.

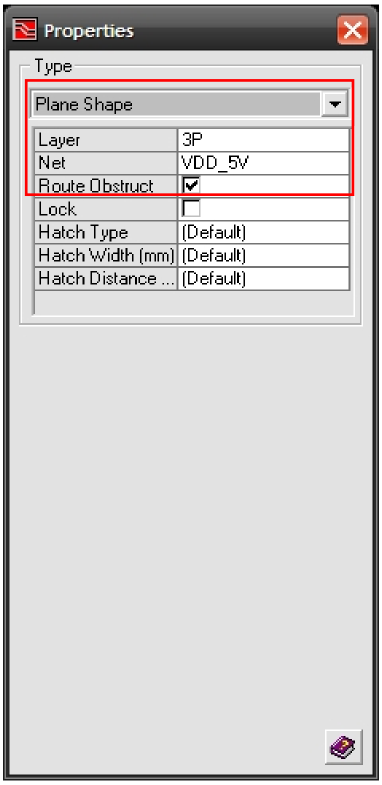


All vias should be located as close as possible to their corresponding pin. If the automatic or manual fanout leaves excess track, click and drag the via towards the pin until the clearance rules block any further motion.

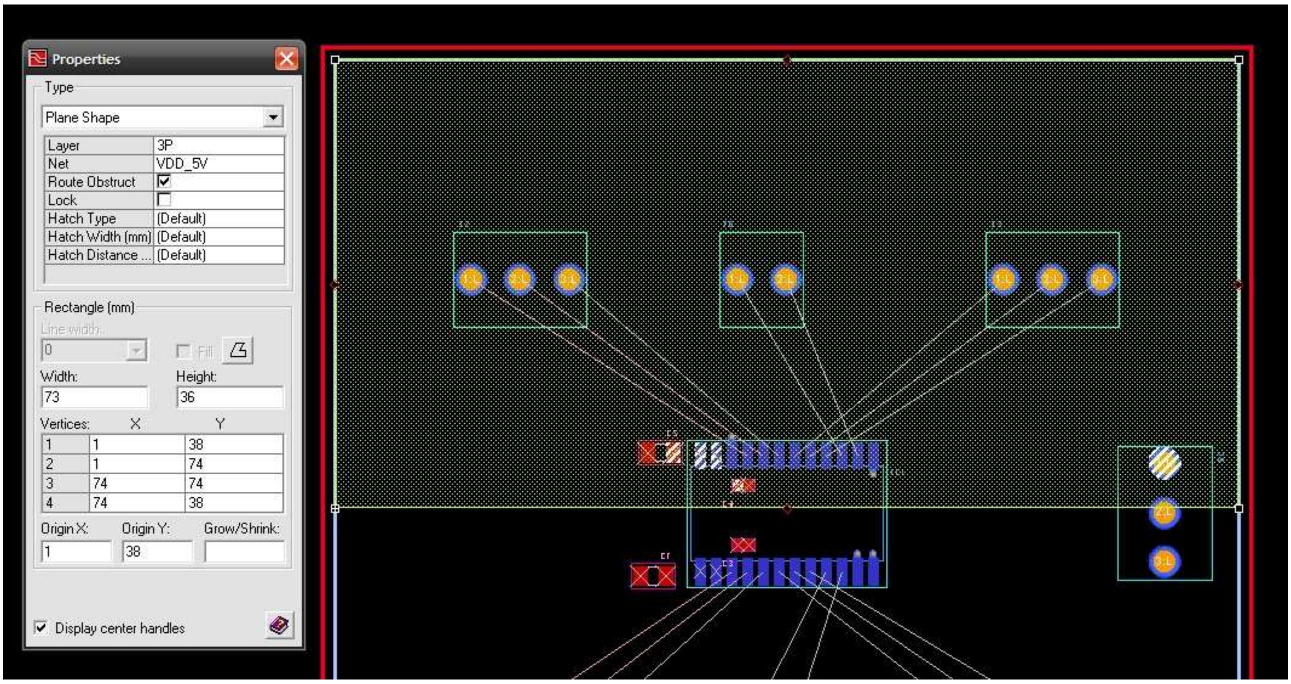
5. In order to fan out a power/ground pin to a plane layer that has been assigned multiple nets, it is first necessary to draw a plane shape for each one. Go to the ‘Display Control’ dialog and ensure that ‘Plane Shapes & Obstructs’ and ‘Fill Plane Shapes’ are both ticked.



Click the ‘Draw Mode’ button on the toolbar, then right click on any empty space and select ‘Properties’ to open the ‘Properties’ window. From the drop down menus, set ‘Type’ to ‘Plane Shape’, specify the ‘Layer’ number on which the object should be drawn, select the ‘Net’ to which the object should be connected and tick the ‘Route Obstruct’ button.

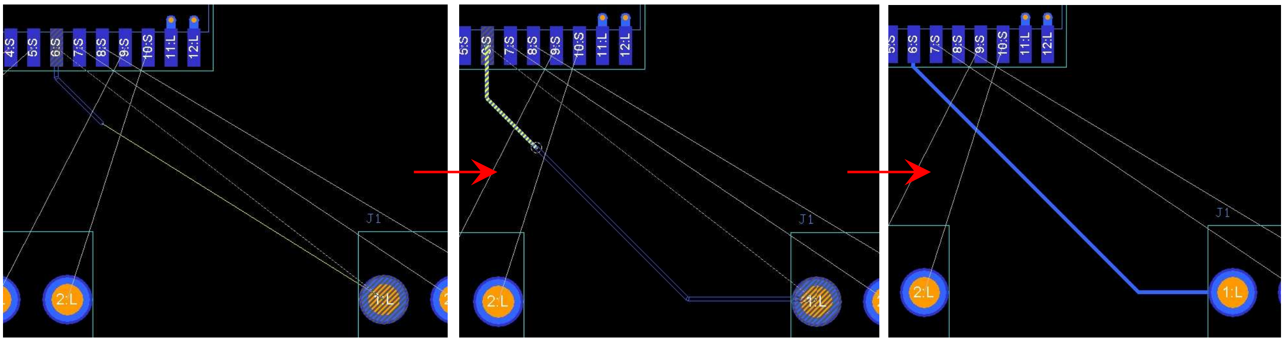


To place the plane shape, press any of the ‘Add Lines/Shapes’ buttons on the toolbar and click/drag within the ‘Route Border’ of the PCB to draw an outline. The dimensions may be set precisely by entering values in the ‘Vertices’ table of the ‘Properties’ window.

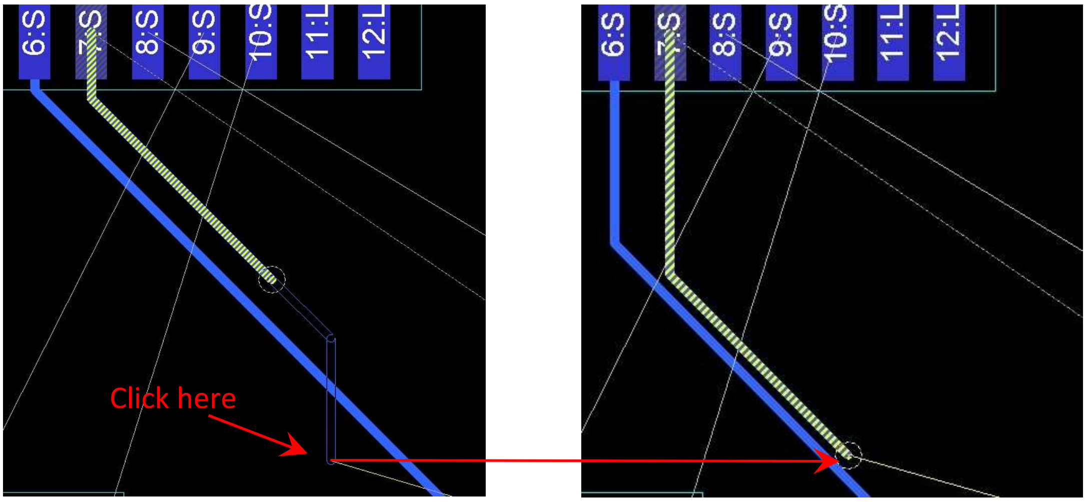


Once all plane shapes have been drawn, return to the ‘Display Control’ dialog and uncheck ‘Fill Plane Shapes’ (the grid pattern tends to obscure other layout operations).

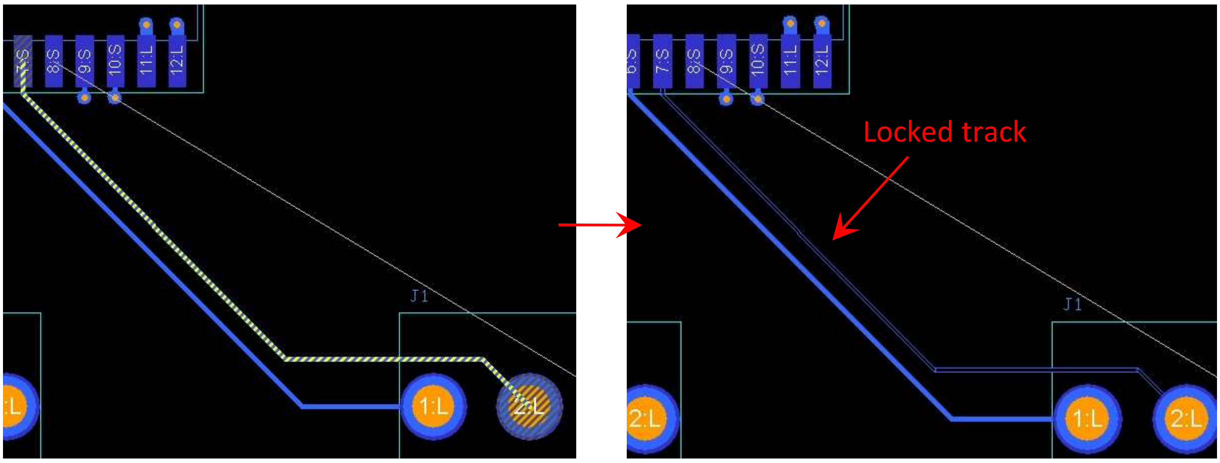
6. The paths of signal nets between pins are indicated by a series of point to point guidelines, referred to as the ‘rat’s nest’ (due to its untidy appearance). To route a track between two pins on the same side of the PCB, press the ‘Route Mode’ button on the toolbar, highlight the first pin and press the ‘Plow’ button (also on the toolbar). The mouse pointer will turn into a track outline and it is then just a matter of following the rat’s nest. Clicking in empty space lays down a track segment (enabling routing around obstacles) and clicking once on the second pin completes the track. Existing routes can be moved simply by clicking and dragging; a track is removed by double clicking to highlight its entire length and pressing the DELETE key.



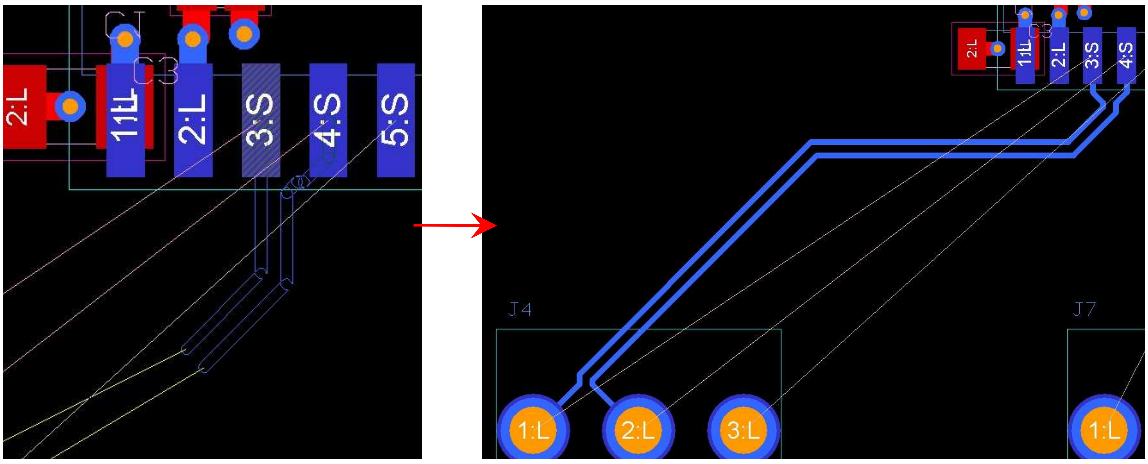
Attempting to route a track over the top of another causes the existing track to be shoved out of the way:



This is often undesirable behaviour, especially when trying to lay tracks as close together as possible in a dense region of a board. To permanently fix the position of an existing track, highlight it with a double click and press the ‘Lock Route’ button on the toolbar (it may be freed again with the ‘Unlock Route’ button).

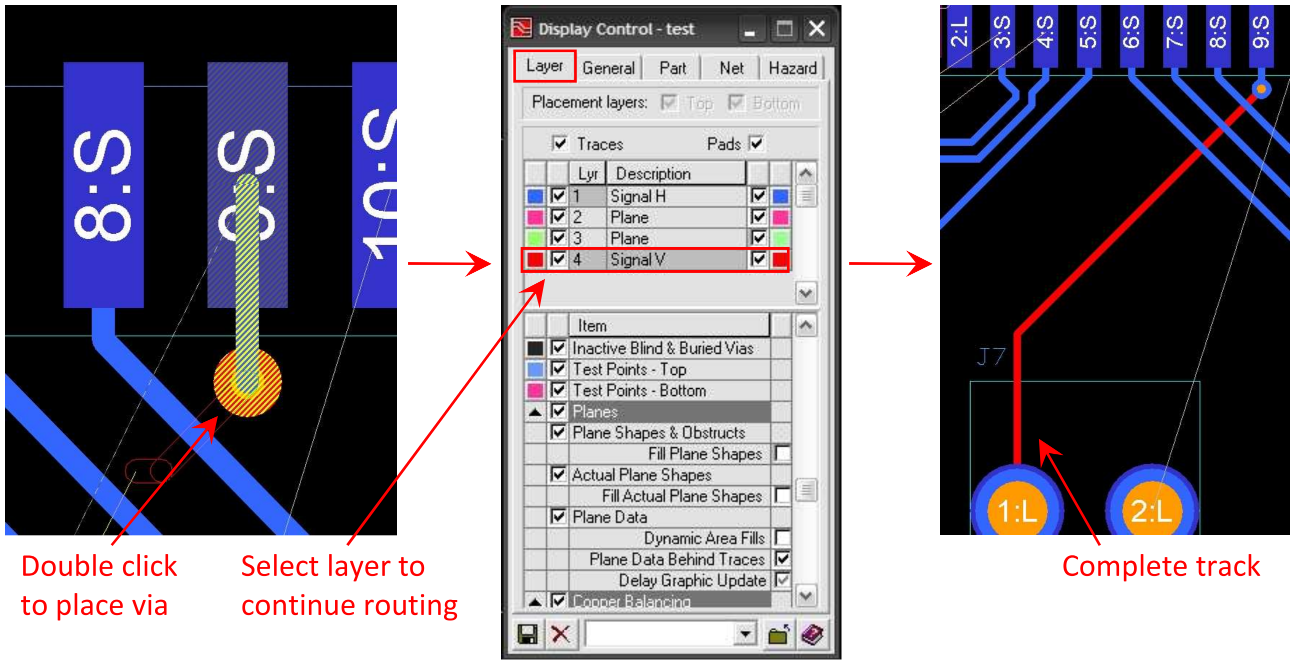


Differential signals (indicated by a pink rat's nest) are a special case. Clicking on one pin of a differential pair and pressing the 'Plow' button starts routing from both pins simultaneously. The twin tracks are maintained at a fixed distance (defined by the net class) and terminating the first automatically completes the second. By default, differential nets always show a form of rat's nest even when they are routed – to switch this off, uncheck the 'Ordered & Routed Netlines' option in the 'Layer' tab of the 'Display Control' dialog.



To route a track from a surface mount pin across multiple layers, it is first necessary to perform a fanout; highlight the pin, click 'Plow' on the toolbar and double click to place a via. From this via (or, indeed, any through hole padstack), the layer for continued routing may be specified by selecting a layer entry in the 'Display Control' dialog (note that placing a via will automatically switch routing to the furthest alternative signal layer). Complete the track on the preferred layer, placing another fanout via at the destination pin if required.

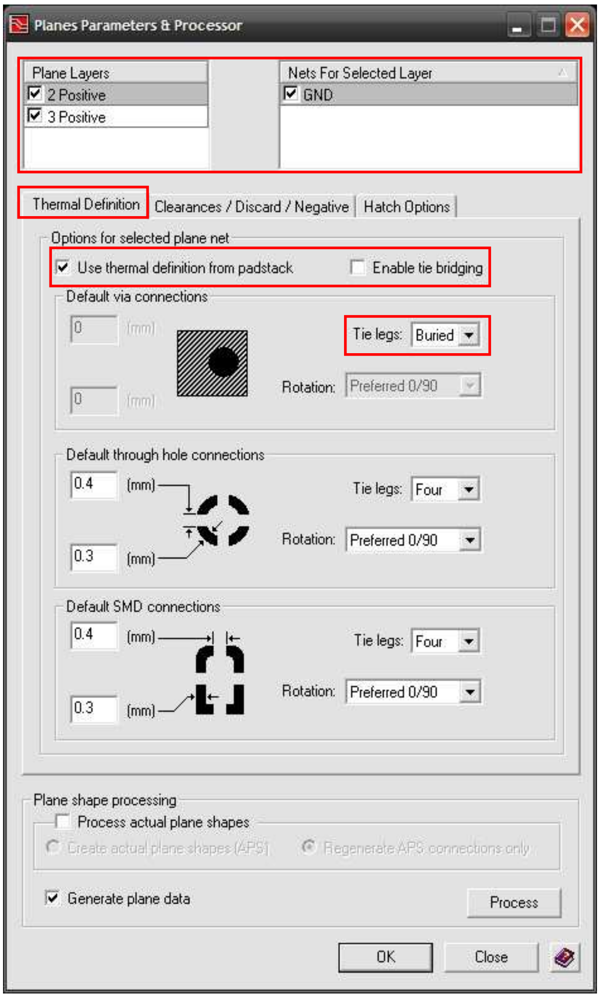
Although it is possible to use an arbitrary number of vias along the length of a track, it is very bad practice to use anything more than a single fanout via at either end (and these should be placed as close to their respective pins as possible).



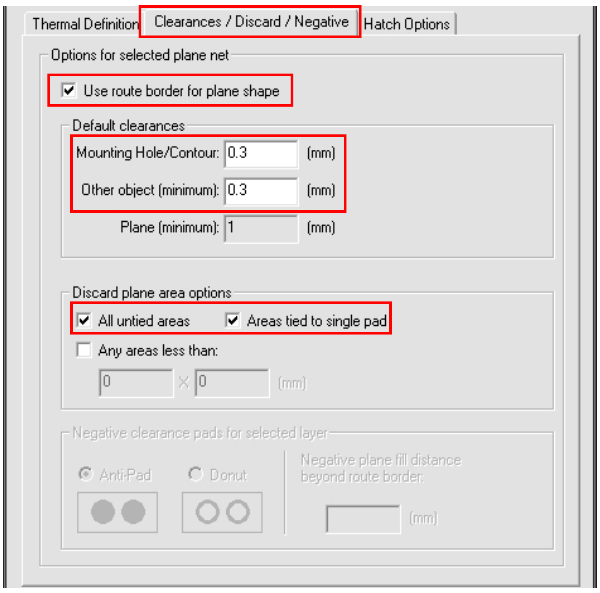
When a net has been routed, it is sometimes beneficial to have Expedition attempt to 'clean' the track by removing unnecessary kinks; this is done by highlighting the track and pressing the 'Gloss' button on the toolbar. If the 'optimisation' leads to unfavourable changes, simply undo the operation.

7. Once all components have been placed and all routing is complete, it is necessary to generate the copper fill areas for any plane layers. Select 'Planes > Planes Parameters & Processor' from the menu to open the 'Planes Parameters & Processor' dialog. The 'Plane Layers' control at the top left of the window lists all layers that contain one or more plane shapes; when a layer is selected, the nets assigned to it are listed in the 'Nets for Selected Layer' control. Ensure that all entries in both lists are ticked. The various tab box settings are configured individually for each 'Nets for Selected Layer' item for each layer, but in most cases it is sensible to use common values for all plane shapes.

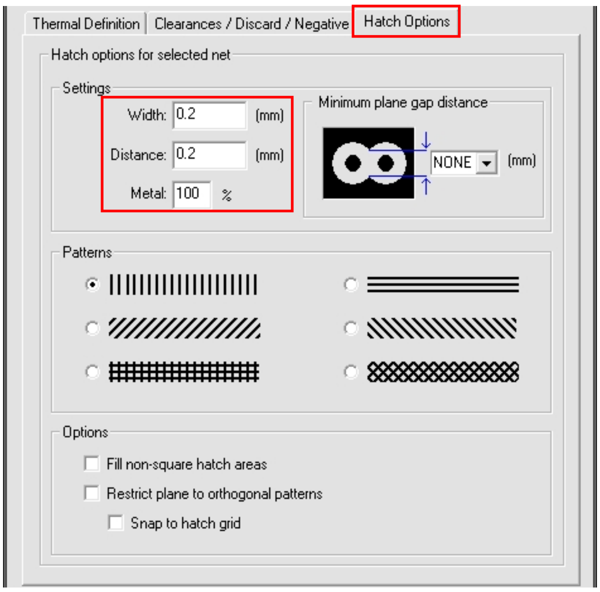
   Select the first layer/net combination and go to the 'Thermal Definition' tab. Tick 'Use thermal definition from padstack' and ensure that 'Enable tie bridging' is unchecked. For the 'Default via connections', it is normal to set 'Tie legs' to 'Buried'. This means that vias connected to the generated plane shape will have no thermal relief, which is appropriate since nothing should ever be soldered to a via. Thermal definitions for 'Default through hole connections' are essentially irrelevant, as each through hole padstack should have been assigned specific 'Plane clearance' and 'Plane thermal' pads at the Library Manager stage. 'Default SMD connections' typically do not require thermal definitions, as it is uncommon to place a surface mount part within a plane shape on the outer layers of a PCB (it is sometimes necessary when designing power supplies – in this case, the thermal ties should be made sufficiently large for the maximum expected current flow to/from the pad).



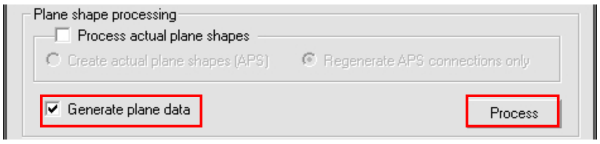
In the 'Clearances / Discard / Negative' tab, the 'Use route border for plane shape' control is set automatically (it is determined by the 'Setup Parameters' configuration discussed earlier). The 'Default clearances' for 'Mounting Hole/Contour' and 'Other object (minimum)' should be determined from the manufacturer's DFM guidelines, but 0.3 mm is typically a 'safe' value. Ensure that 'All untied areas' and 'Areas tied to single pad' are ticked in the 'Discard plane area options' section; this facilitates the identification of any errors in the generated output.



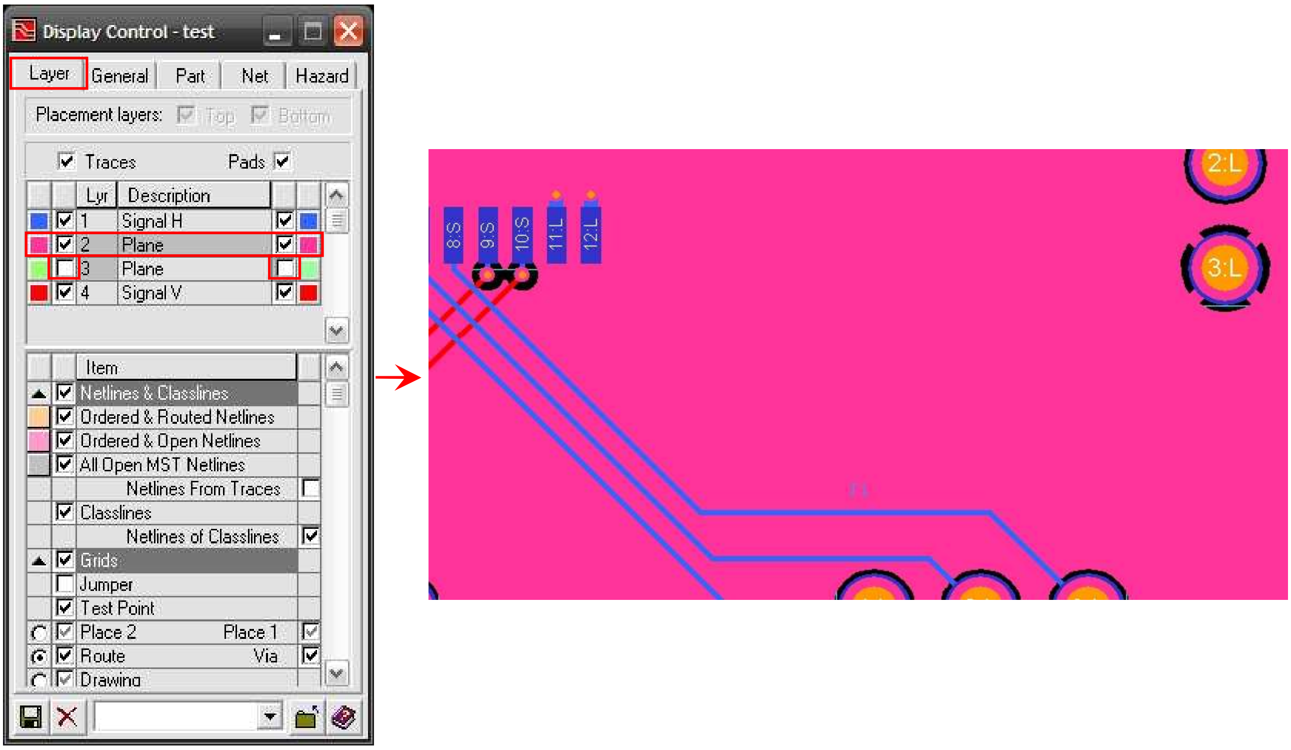
The copper fill that defines the plane shape is actually a hatch pattern comprised of a series of lines. In the ‘Hatch Options’ tab it is necessary to enter appropriate values for the ‘Width’ of the lines and the ‘Distance’ between them. These values should be equal to ensure 100% copper coverage. The width must be small enough for the individual hatch lines to fit between the various through hole pins and vias on the PCB – 0.2 mm is typically adequate.



Once the above configuration process has been repeated for all layer/net combinations, ensure that ‘Generate plane data’ is ticked and press the ‘Process’ button. A pop up message will appear when the operation is complete, and the plane shapes on the PCB itself will be filled with a block colour representation of the hatch pattern.



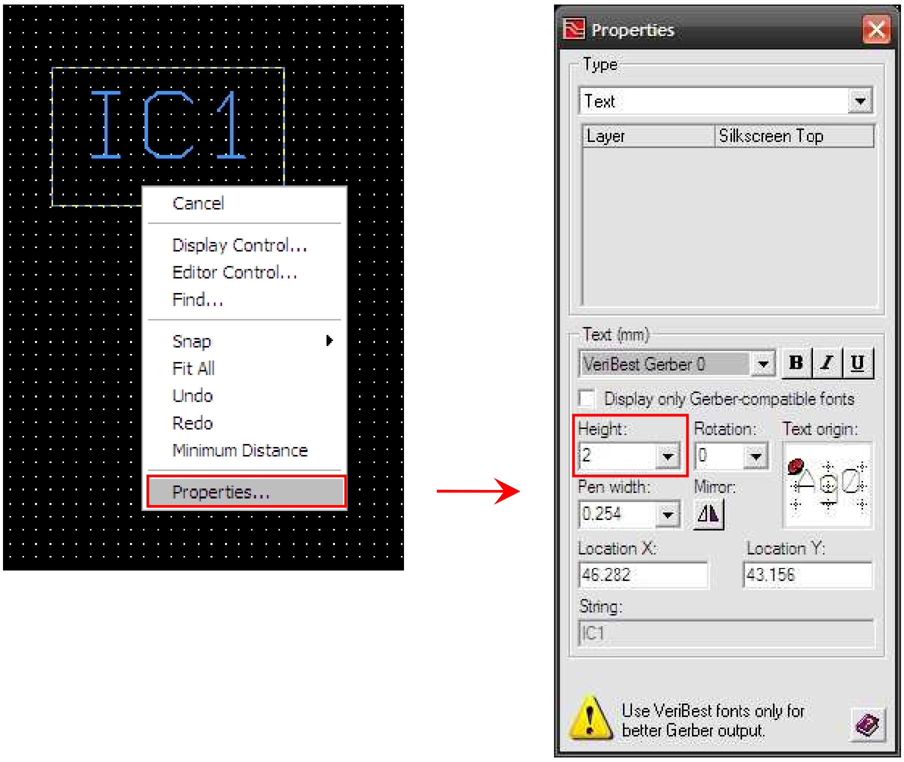
It is beneficial to visually inspect the generated plane shapes for errors. Go to the ‘Display Control’ dialog and select the first plane layer. Hide the other planes by unchecking the tick boxes either side of their entries in the list. Vias connected to the plane net should be embedded in the shape, whereas connected through hole pins should be joined via cross shaped thermal pads; everything else should be clearly isolated. Unexpected holes in the plane shape may indicate that vias are placed in too large and tight a conglomeration (thus creating a barrier to current flow in all planes), or the hatch width is too large. Repeat the check for each of the remaining plane layers.



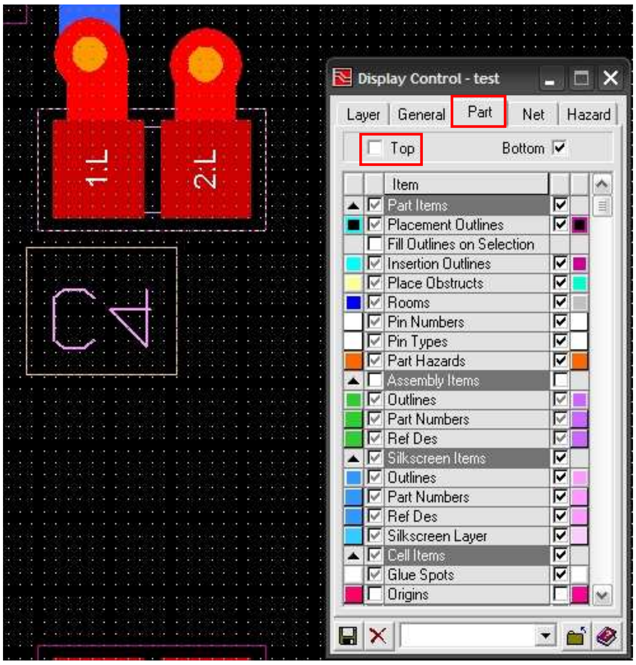
It is important to note that the plane shapes are not updated automatically when components or vias are moved. If the layout is ever changed, the plane shapes must be regenerated by again clicking the 'Process' button in the 'Planes Parameters & Processor' dialog.

Once the plane generation is complete, all plane layers may be hidden: select the first signal layer in the 'Display Control' dialog and uncheck the tick boxes either side of each plane entry.

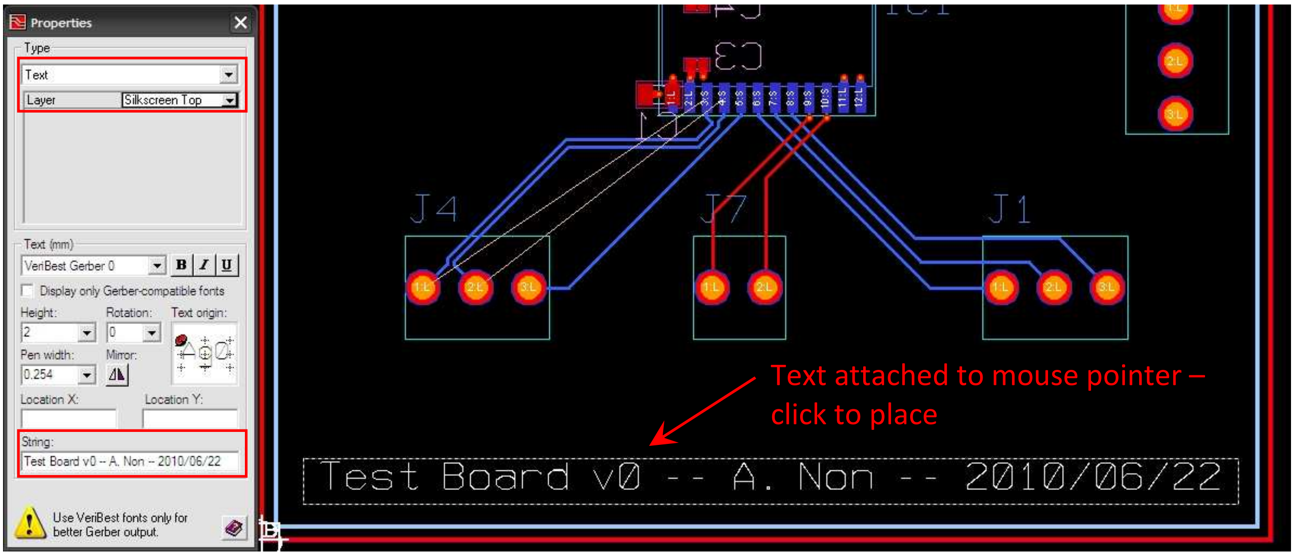
8. The most significant remaining aspect of the PCB design is typically silkscreen generation. Arguably the most important items on the silkscreen are the component reference designators, and it pays dividends to spend time ensuring that reference designator text is accurately placed (rotating a part can move the text to unexpected locations…) and readable. Click the 'Draw Mode' button on the toolbar, right click one of the reference designators and select 'Properties' to open the 'Properties' dialog. The text 'Height' should be at least 2 mm (1 mm is acceptable for very tight layouts) – there is no upper limit. To move text, simply click and drag; the F3 key rotates selected text in 90° increments. The reference designators should be placed close to their respective components, with ~0.1 mm offset from any pads and ~0.3 mm offset from any silkscreen part outlines.



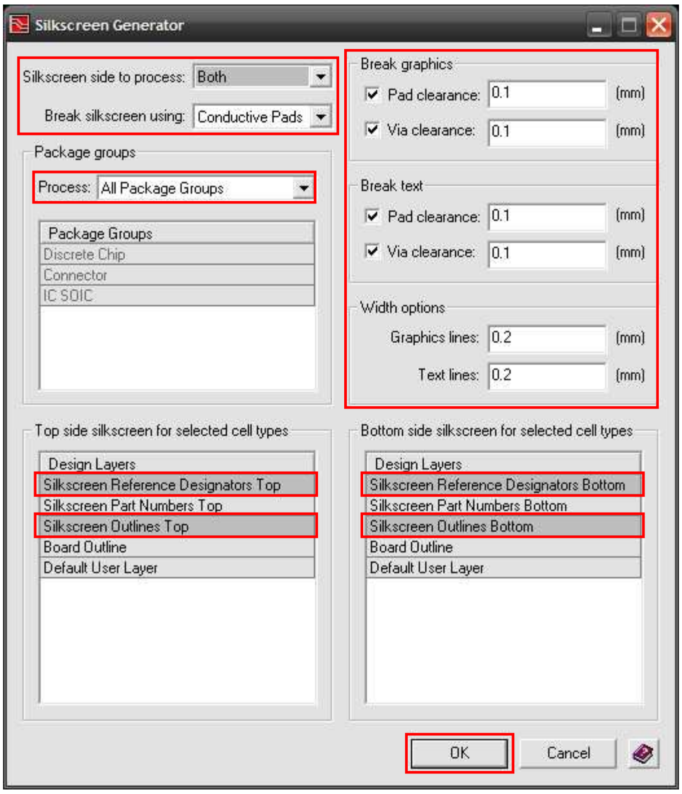
If text on the bottom layer of the PCB is obscured by drawing objects on the top, simply go to the 'Part' tab of the 'Display Control' dialog and temporarily uncheck the 'Top' item.



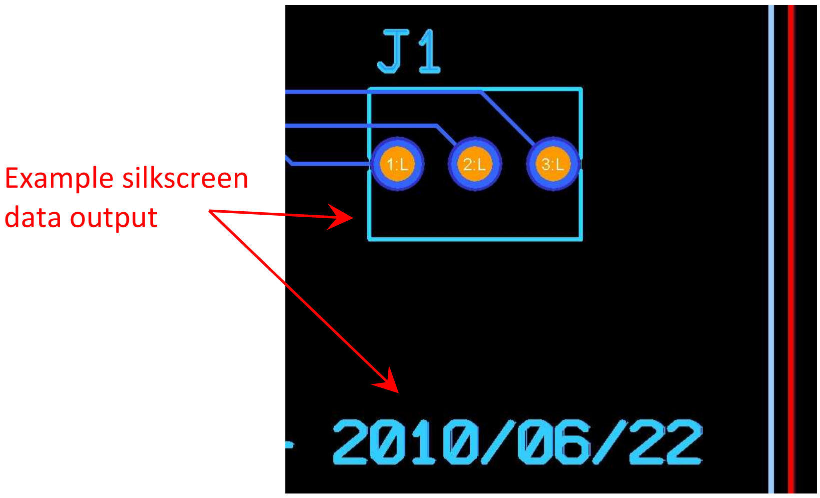
It is also customary to add a silkscreen label to the PCB identifying the board name, designer and completion date. To do this, press the 'Add Text' button on the toolbar to again open the 'Properties dialog'. 'Type' will be set to 'Text', and 'Layer' should be changed to 'Silkscreen Top'. Enter an appropriate label in the 'String' box and it will automatically become attached to the mouse pointer – click anywhere on the PCB to place the text.



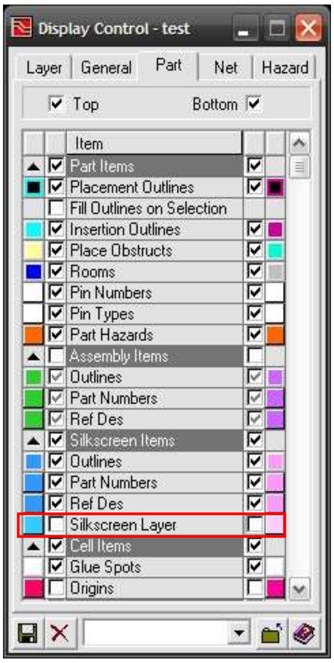
All of the silkscreen drawing objects are in fact place holders. To actually produce the silkscreen data, select 'Output > Silkscreen Generator' from the menu to open the 'Silkscreen Generator' window. Configure the dialog as in the following screenshot and press the 'OK' button:



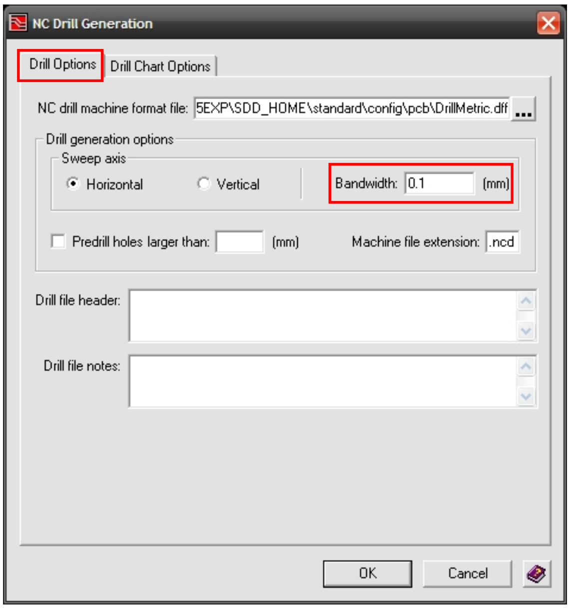
A pop up message will appear when the operation is complete, and an overlay of the result will be displayed on the PCB layout. As with plane shapes, silkscreen data are not automatically updated when the design is modified – if any text or part outlines are changed, it is necessary to rerun the 'Silkscreen Generator'.

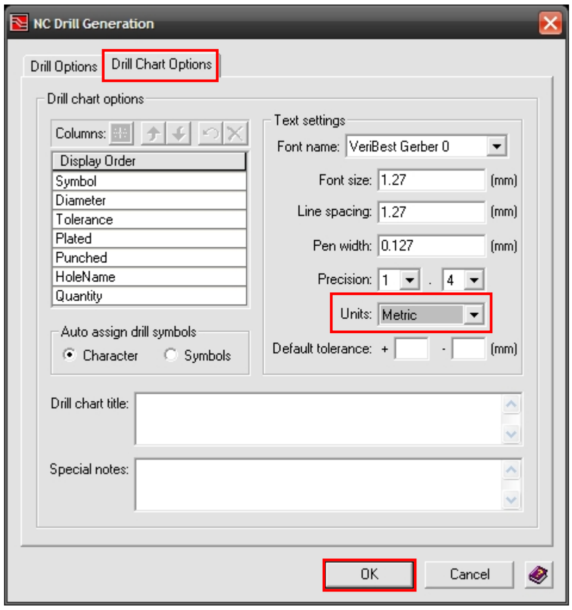


Note that displaying silkscreen data can require an enormous amount of memory – if the performance of Expedition is affected, hide it by unchecking the tick boxes either side of the 'Silkscreen Layer' entry on the 'Part' tab of the 'Display Control' dialog.

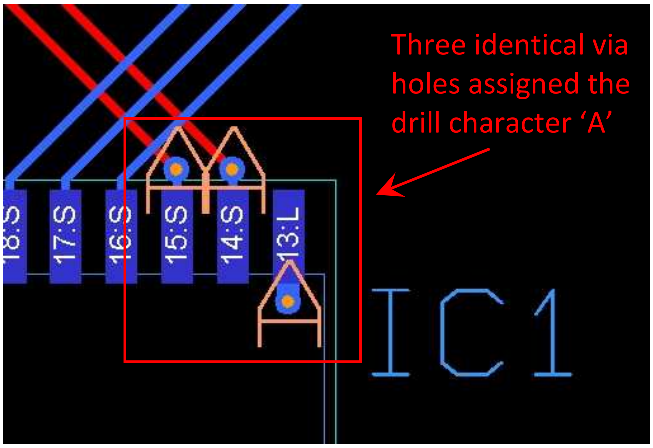


9. The final step of the design is generation of the drill drawing (note that this is not strictly required, but it enables easy access to the drill information that must be included when requesting manufacturing quotes). Select 'Output > NC Drill…' from the menu to open the 'NC Drill Generation' dialog. On the 'Drill Options' tab set 'Bandwidth' to 0.1 mm and on the 'Drill Chart Options' tab set 'Units' to 'Metric' – all other options may be left at their default values. Press the 'OK' button to begin generation.





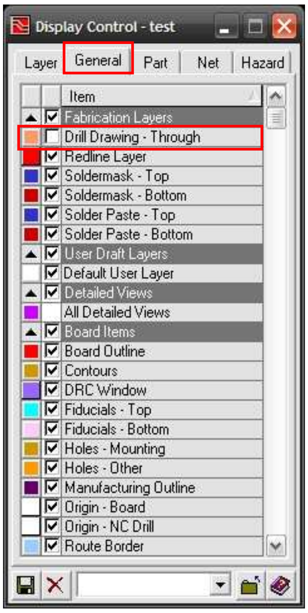
When the operation is complete, a drill drawing layer will be added to the board display. Each hole will be assigned a character according to its size…



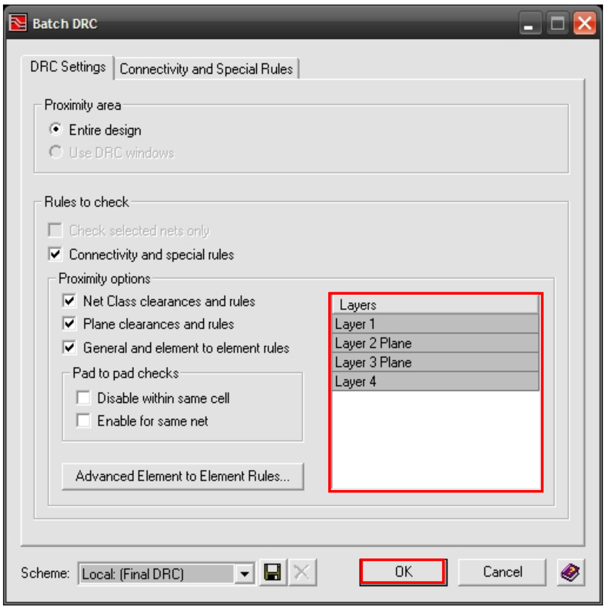
…and a table summarising all hole parameters will be displayed beneath the PCB.

Through Holes						
Symbol	Diameter (mm)	Tolerance (mm)	Plated	Punched	Hole Name	Quantity
A	0.3000		Yes	No	Rnd 0.3	16
B	1.8000	+/- 0.0500	Yes	No	Rnd 1.8 +/-Tol 0.05	19

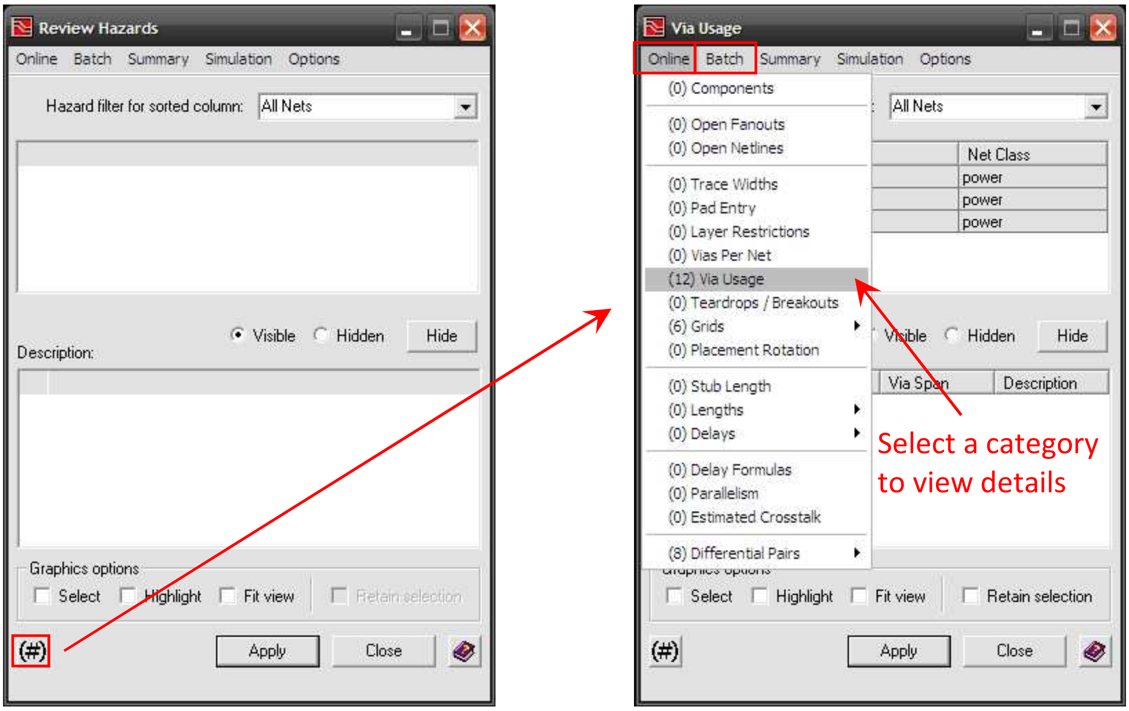
As with plane shapes and silkscreen data, the drill drawing must be regenerated each time the design is modified. To hide the drill information (this is recommended, as it clutters the display), go to the 'General' tab of the 'Display Control' dialog and uncheck the 'Drill Drawing – Through' entry.



10. Once a design is complete, it should be checked for errors. Select 'Analysis > Batch DRC…' to open the 'Batch DRC' dialog (DRC = Design Rule Check). The default options are correct; simply ensure that all entries are highlighted in the 'Layers' list and press the 'OK' button.

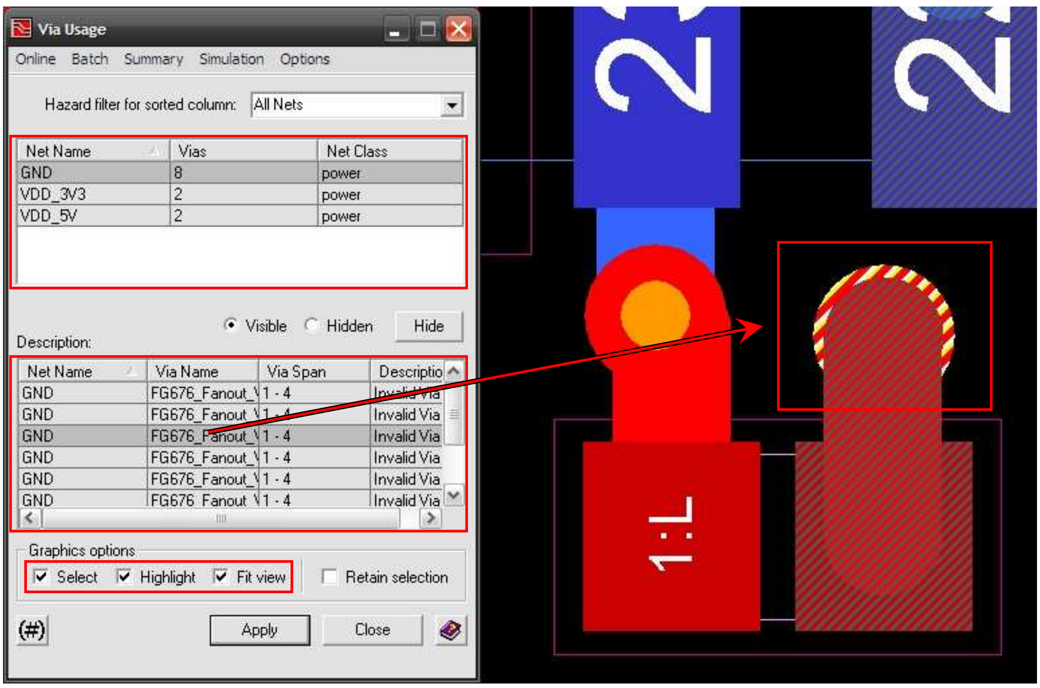


When the operation is complete, select 'Analysis > Review Hazards…' to open the 'Review Hazards' dialog and click the '(#)' button to load the latest batch DRC results. Errors may then be viewed by category from the 'Online' and 'Batch' drop down menus (the integer next to each category indicates the number of detected problems).



Selecting a category fills the upper table with a list of affected nets. Highlight a net entry to display a list of specific error instances in the lower table. If the ‘Select’, ‘Highlight’ and ‘Fit view’ options are ticked, double clicking an error will focus the PCB view on the problem area.

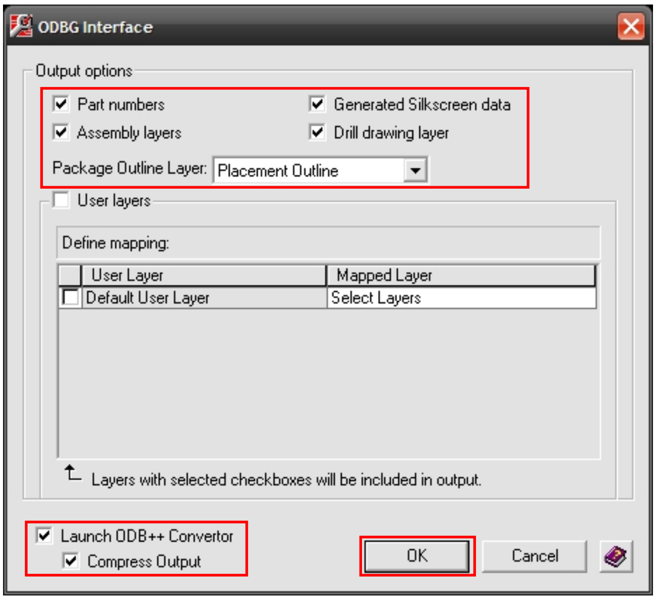
It is the designer’s responsibility to manually check and correct each ‘hazard’. In some cases, highlighted problems will actually result from deliberate design choices. For example, the following screenshot demonstrates an ‘Invalid Via’ error for a particular ground net fanout; this originates from the fact that the designer specifically chose to use a via padstack different from the net class default. These ‘false positive’ warnings should be ignored.



Generating Manufacturing Files

PCB manufacturers typically require a design in either Gerber or ODB++ format. The latter is universally favoured and should be used wherever possible (the files are easier to handle and tooling costs are reduced). Expedition cannot natively produce ODB++ files; it exports data in 'ODB Gateway' format and an external 'GW2ODB' plug-in performs the conversion to ODB++. GW2ODB must be installed independently from the Mentor Graphics software package – an installer (gw2odb_setup_v750.exe) may be found in the 'Utilities' folder of the 'PCB_Notes' Google Docs area.

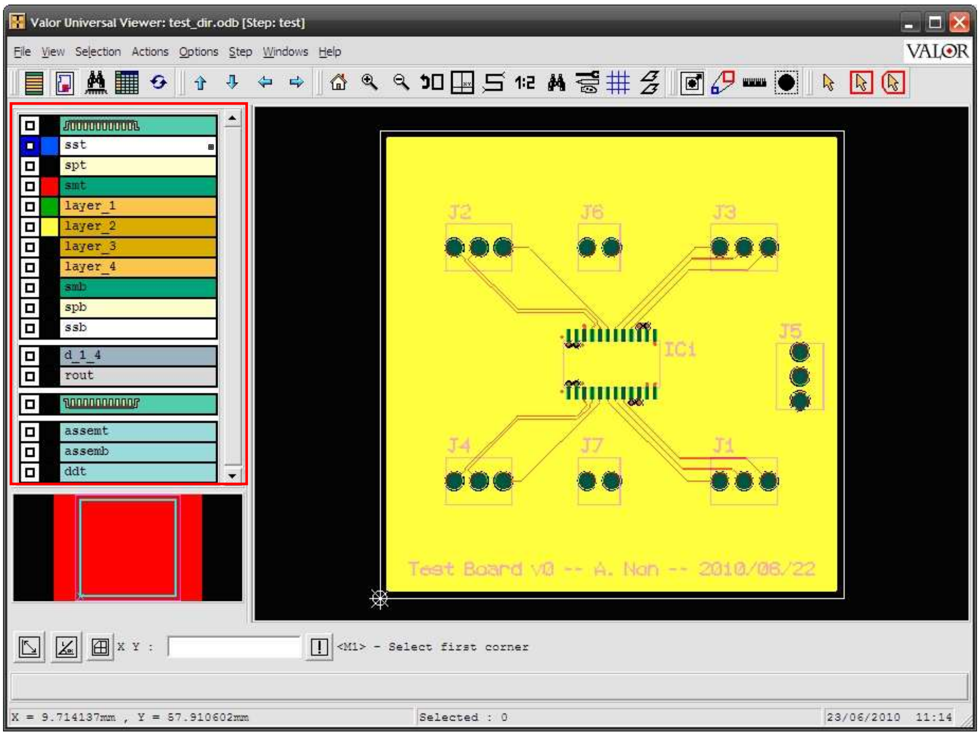
To generate an ODB++ file from a design, first open the 'ODBG Interface' dialog by selecting 'Output > ODBG Interface…' from the menu. Configure the various options as in the following screenshot and press the 'OK' button: (note that the ODB++ converter settings are only enabled once GW2ODB is installed)



If successful, the dialog will close silently. The output file has the path:

<*project_directory*>\PCB\Output\<*project_name*>_dir.odb.tgz

It is good practice to visually inspect the generated ODB++ data before submitting it to a manufacturer. The only available freeware ODB++ viewer is the 'Valor Universal Viewer' (VUV) – an installer for this (vuv_732.exe) may also be found in the 'Utilities' folder of the 'PCB_Notes' Google Docs area. Run VUV, open the .odb.tgz file and select which layers to view from the panel at the left hand side of the window (up to four layers may be shown at once). Particular attention should be paid to via/pad connections and clearances on the plane layers (this serves as a final check that the user remembered to update the generated plane data following any changes to the layout).



Requesting a Quote

Once the design is complete and verified, a request for a quote should be sent to the manufacturer. This should contain the following details:

- PCB Name
- Board size *(in mm)*
- Number of layers
- Hole count *(per board)*
- Board thickness *(in mm)*
- Min drill *(minimum hole size, in mm)*
- No. of drill sizes (*number of different hole sizes)*
- Material *(laminate material)*
- Resist side (*the number of sides that require solder resist: 0, 1 or 2)*
- Resist Colour *(the colour of the solder resist)*
- Silkscreen quantity *(the number of sides that have silkscreen items: 0, 1, or 2)*
- Silkscreen colour
- Surface finish *(the coating applied to exposed copper areas)*
- Supply *(specifies whether boards are supplied individually or in a panel)*

The quote request should include any controlled impedance track width and gap information provided by the manufacturer, and a copy of the generated ODB++ file. When stating how many boards are required, also specify the desired leadtime (always ask for a range of quantities with several leadtimes, as the most cost effective option is not always obvious).

A number of the above details have standard values which should be appropriate for all MICE work:

- Board thickness: 1.6mm
- Material: High Tg FR4
- Resist side: 2
- Resist Colour: Green
- Silkscreen quantity: 2
- Silkscreen colour: White
- Surface finish: Immersion gold
- Supply: As circuits

Note that the term ‘circuit’ is often used interchangeably with ‘board’ in the context of a quote.

For reference, an example of the type of email request that should be sent to a manufacturer is given below:

```
Could you please give me a quote for the following PCB:

Name: MICE Target Interface Board
Board size: 100mm x 100mm
Number of layers: 8
Hole count:  522 per circuit
Board thickness: 1.6mm
Min drill: 0.3mm
No. of drill sizes: 6
Material: High Tg FR4
Resist side: 2
Resist Colour: Green
Silkscreen quantity: 2
Silkscreen colour: White
Surface finish: Immersion gold
Supply:  As circuits
Controlled Impedance: 50ohm single-ended on all tracking layers, with build and
track widths as recommended by Mike McMahon (see
BuildAndTrackWidthsFromExpressCircuits.pdf, attached)

I have also attached an ODB++ file for the board:
micetargetinterfaceboard_v0_dir.odb.tgz

If possible, I would like quotes for:

2 circuits - 5 days lead time
4 circuits - 5 days lead time

2 circuits - 10 days lead time
4 circuits - 10 days lead time

Please do not hesitate to contact me if you require any further information.
```

Ordering PCBs

One final additional step is required when accepting a fabrication quote and completing the order: ask the manufacturer to add ‘copper balancing’ to the signal layers of the board (this prevents the PCB from warping, and should not affect the cost).